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Woods Hole Oceanographic Institution

High Continuous Bandwidth Multichannel Acquisition System

by

Keith von der Heydt

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Technical Report

Funding was provided by the Office of Naval Research
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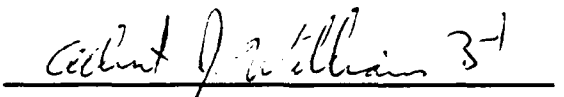

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High Continuous Bandwidth Multichannel Acquisition System

Keith von der Heydt
Woods Hole Oceanographic Institution

June 12, 1991

1 Abstract

Multichannel data acquisition has been a keystone of 7 ONR sponsored Arctic acoustic research programs conducted jointly by WHOI and MIT investigators from 1978 through 1989. This report describes the status and capability of the most recent system developed at WHOI for the purpose of acquiring digital data from up to 64 channels at sampling rates up to 20 kHz per channel with data bandwidth to 5120 Hz. ONR funded the development of and use of this system and its prototype for 2 Arctic field experiments, PRUDEX 87 and CEAREX 89. It was most recently used during the Heard Island Feasibility Experiment in February 1991. Of note are *the auto-gain ranging capability offering a dynamic measurement range of greater than 120 dB*, the continuous storage capability of up to 200,000 samples per second to a Small Computer System Interface (SCSI) device, typically optical disk, and easy expandability with additional identical channels connected in parallel.

Contents

2 Introduction

The techniques for doing multichannel seismic work in science and industry have usually focused on high dynamic range and high speed acquisition for short periods. The intermittent nature of reflection and refraction data acquisition often permits a system to buffer incoming data in memory for the duration of an event and store it to an archiving medium between periods of data generation.

Our acoustic work has required multichannel data acquisition at bandwidths similar to seismic applications but for extended periods (hours). We have developed a system of modest cost that offers both the high dynamic range capability often required of acoustic and seismic systems and high continuous storage bandwidth to a medium that affords easy access during processing.

This report describes the features of a system that has satisfied these requirements. The work has come about as a function of scientific needs of our joint MIT/WHOI Arctic acoustic work. The trend, as might be expected, has been to more channels, higher signal bandwidths and the ability to deal with greater volumes of data. Thus an objective has been to design acquisition systems that are expandable and have data generating capabilities consistent with that of practical storage devices. As it becomes easier to acquire large data sets, increasing emphasis must be placed on the need to monitor and verify data quality in near real-time to minimize the chance of returning from an experiment with bad data.

Three sections are presented in this report:

1. A discussion of and documentation regarding the Gain Ranging Amplifier (GRA) developed for use during ONR sponsored Arctic acoustic research programs at WHOI

2. A discussion of and documentation describing the multichannel acquisition hardware and software developed to store data generated by a bank of parallel GRA's. An update to WHOI Technical Report #87-49 regarding storage formats used for data on the optical disk is included.

3. Some thoughts on future data acquisition efforts

3 The Gain Ranging Amplifier

We have been involved with projects having data acquisition requirements focused on high dynamic range digital recording of seismo-acoustic signals. The character of such signals often includes explosive events, widely varying backround noise that can mask signatures of interest, and generally unpredictable conditions.

In this discussion, the term *dynamic range* refers to the range of signal amplitudes over which the system can automatically adjust to prevent overloading and represent with the combination of a 13 bit analog-to-digital converter word and a 3 bit gain word. We are using the term *dynamic range* synonomously with system *measurement range* to describe the difference in spectral level between the maximum signal that can be represented and the noise floor of the system. This we distinguish from the 13 bit binary *precision* of the system

used to quantize each sample of the signal. These definitions are confused by the "floating point" nature of a ranged system whereby a sample value is represented by a "mantissa" of 13 bits with binary resolution and an "exponent" of 3 gain bits with factor-of-8 resolution. In fact, in the presence of a large amplitude in-band signal, the representation of a second smaller in-band signal is limited to the 13 bit *precision* of the "mantissa".

Similar to the seismic industry, we developed (at lower cost), auto-ranging amplifier techniques that provide very high ($> 130dB$) measurement ranges by instantaneously selecting the optimal available gain for a signal prior to digitizing a sample and including that gain as part of the sample value. Effectively, this technique shifts the precision of the analog-to-digital converter over the available measurement range determined by the noise floor of the system.

The chief benefit of a GRA, or floating point amplifier, is that one can be largely unconcerned with the dynamic range of the signal to be digitized, while being assured that a sample will be represented by enough active bits to be useful. As a signal varies in amplitude, the gain is determined at sample time. The rate of gain change is a function of sample rate relative to the instantaneous rate of change of the signal. The gain at which a sample is taken, together with the output of the analog-to-digital converter, become the sample value. This is usually an acceptable compromise compared to having a precision of 24 bits.

Our approach has been to use a distributed system that has complete filter, amplifier and digitizing functionality per channel whose digital output can be accessed via a common bus with as many other channels as are necessary. This parallel approach is convenient because there is no sampling skew in time for any number of channels, (simultaneous sampling is assured), and the number of channels can easily be increased up to the available bus bandwidth.

3.1 Hardware

Previous GRA designs developed by the author employed both gain switching and gain decision algorithms. Distinction is made here between gain switching and gain decision auto-ranging methods. Gain switching, in this discussion, refers to a "discrete" gain control whereby a single amplifer has its gain changed to one of a set of fixed possibilities for every sample. Gain selection refers to having the signal at multiple gains available at all times and selection of the most appropriate gain range for digitization is made based on amplitude and slew considerations.

These designs suffered from 1 of 2 problems:

- A single amplifier had its gain changed by switching 1 or more resistors in the gain control network. This scheme can be prone to overload upon reception of fast, high amplitude signals when at a high gain. Our experiments often have the combined requirement of recording signals below the ambient noise level as well as signals from explosive and other impulsive sources. The low pass anti-alias filter used prior to the switched amplifier limits the rise time of such signals, but in practice is unable to prevent overloads under some conditions.

- Gain decision methods can prevent any possibility of overloaded samples (except when the front end itself is overloaded). This technique however, can exhibit significant harmonic distortion not only due to gain differences at each range (similar to switched gain method above) but to offset differences and skew between ranges.

Numerical modeling of the gain selection method showed that the most important source of harmonic distortion was the difference in DC offset among gain ranges. This led to use of a processor controlled amplifier that allows digital nulling of the offset from each sample, based on a stored offset value measured at that gain range. With amplifiers having nominally a low DC offset, there is then no need to null individually the offset at each gain range since it is automated.

The functional description of the GRA we have developed, Figure 1, is the following:

- DC coupled, fixed gain single ended amplifier with software programmable gains of 0 through 42 dB in 6 dB steps
- software selectable and resistor pack programmable 4 pole highpass Butterworth filter
- software programmable, low pass 8 pole Butterworth filter, 20 to 5120 Hz in 20 Hz steps
- .01 Hz AC coupled bank of 5 cascaded amplifiers with outputs at gains of 1, 8, 64, 512 and 4096; (the bank is AC coupled, stages are DC coupled)
- A 13 bit self calibrating analog-to-digital converter (ADC) at each gain range
- An 87C51 microcontroller that selects the optimal gain range, corrects samples for DC offset, makes data available to the bus when the card is addressed, and enables channel configuration via serial communication with a "host"

The diagram of Figure 1 shows the functional elements of the GRA. Figure 39 is a photograph of the GRA card and Figure 40 is the schematic of the design. An input signal is AC or DC coupled with a jumper at the input to an on-board, fixed gain, single ended input preamplifier (PA). From the output of the PA, the signal passes either directly or via a 4 pole Butterworth highpass filter (HPF), to the 8 pole Butterworth lowpass filter (LPF). The HPF is resistor programmable and its use is software selectable. The LPF is software programmable in 20 Hz steps from 20 through 5120 Hz. The output of the LPF is connected to a unity gain amplifier and a series of 4 cascaded amplifiers via a buffered .01Hz AC coupling. The coupling eliminates the DC offset at the output of the LPF. Each of the cascaded amplifiers has a fixed gain of 8, providing individual copies of the bandlimited input signal at gains of 1, 8, 64, 512, & 4096. Each of these signals is applied to a separate ADC converter working from a common voltage reference. At each sample period, all 5 ADC's generate a 13 bit word from which the 87C51 controller selects one for output to the system data bus when that channel's address appears on the system address bus.

3.2 The Gain Ranging Amplifier Design Topology

The GRA functional diagram in Figure 1 consists of 6 sections: input buffer amplifier, optional highpass filter, lowpass filter, cascaded amplifier chain, bank of 5 ADC's and controller. Each section will be described in detail.

3.2.1 Front End

In our experience it has often been necessary to distribute sensor signals to more than one recording system. We have chosen to provide separate, low noise single or differential input amplifiers that have multiple, individually buffered outputs. This led to a single ended input on the GRA card. A PA has its fixed gain set under software control to be as high as possible for the expected maximum input signal to avoid the noise floor of the LPF. Figures 2 and 3 with fixed gains of 1 and 16 respectively show the effect of PA gain on the effective system noise floor. There is little decrease in the level of the noise floor using PA gains greater than 16.

3.2.2 Highpass Filter

The highpass filter is used to limit low frequency motion, often of very high amplitude, from hydrophone sensors when towed or suspended in water. Its noise contribution is unimportant compared to that of the lowpass filter.

3.2.3 Lowpass Filter

A software controlled switch is connected such that the input to the LPF can be selected from the either from the HPF, or directly from the PA or to ground during offset calibration periods.

The LPF is a large Frequency Devices module, M/N 848P8B, with noise specified at 50 μvolts over the band 5 Hz to 50 kHz. This broadband noise floor sounds a bit more ominous than it is, as can be seen in Figures 7 through 13 showing noise at various signal levels. (The spectral levels indicated are very close to "per Hertz" normalization because the FFT bin bandwidth is almost 1.) Clearly, the LPF was a design compromise between achieving filter cutoff programmability and a reasonable noise level. The system noise floor is dominated by this filter and it is due to the bi-quad, op-amp intensive configuration of the filter design. These op-amps, TL084's, are moderate in bandwidth but not particularly low in noise level and at this time somewhat aged. These filters were the best available when this card was designed in late 1988.

The rolloff rate of the LPF is 48 dB/oct, samples of which are shown in Figures 4, 5, & 6. The phase and gain match of these filters is $\pm 2.0^{o}$ and $\pm 0.2dB$, max. Distortion from the LPF, $0.004\%(-88dB)$ max, is low compared to the distortion as a function of the gain-ranging technique which will be discussed later. These modules, about $250 each in small quantities, are a significant part of the total cost of a card.

3.2.4 Offset Cancelation

The AC coupling following the LPF is used to minimize the DC offset applied to the cascaded amplifier chain. We are often interested in very low frequency signals hence this coupling resides at .01 Hz via a 470 μf aluminum electrolytic capacitor and a 33.2k metal film resistor. The leakage current of these capacitors is specified at about 15 μV max but in practice it is orders of magnitude lower, making them effective in this application. The objective is to prevent the offset in the amplifier chain from using a significant portion of the $\pm 10V$ swing available at the higher gain outputs. Most of the remaining offset is subtracted out numerically by the controller. This will be discussed later. A side effect of the very low cutoff of the AC coupling is that it takes a few minutes to allow the offset calibration process to arrive at a "quiescent" level after amplifier turn-on.

3.2.5 Auto-Ranging Amplifier

The cascaded amplifier method was chosen because it offers a gain selection method rather than a gain switching method, eliminating the possibility of overload due to inadequate auto-ranging rate. At high signal levels, the higher gain amplifiers are in saturation but quickly recover when the signal decreases. The choice of opamp here is important. Some amplifiers exhibit particularly disagreeable behavior when subjected to abuse such as this. The Linear Tech 1007's have sufficient gain-bandwidth and slew rate to give minimal skew from one gain selection to the next. Their voltage noise level is very low and current noise is not an issue as the source impedances are also low. An important feature is that the controller selects the gain stage to use based not only on whether its level is within scale but also on having been on scale for a minimum number of previous samples. The amplifiers in the chain are DC coupled. Indvidual offset nulling is not necessary because of both the low initial offset of the devices and the dynamic nulling described below.

3.2.6 Analog to Digital Conversion

The ADC's are MicroLinear 2230's, atypical in that they are 12 bits plus sign, have an on-board S/H function and are self calibrating. Unfortunately, they draw about 200 mw from $\pm 5V$ power rails. The input swing is specified at $\pm 5V$ but they can withstand $\pm 12V$ swings without damage. The 13 bit word from this part fits conveniently into a 2-byte sample width when 3 bits are used to specify the gain at which the sample was taken.

3.2.7 Controller

An 87C51 micro-controller provides the following functions:

- configuration capability via an onboard UART
- implements various test and diagnostic modes

- runs offset calibrations
- makes the gain selection after all ADC's sample
- numerically nulls the offset in the selected sample based on a stored measured offset value for each gain range
- makes the sample available on the interface data bus

With a 12 MHz clock, the controller can process a sample in 43 μs. The ADC's sample in 32 μs (about 30 kHz). If a 16 MHz clock was used, the controller would be perfectly matched with the ADC. At 12 MHz, the maximum sampling rate of the GRA is about 22 kHz which is more than adequate with the maximum bandwidth of 5120 Hz from the LPF. Typically we use a sample rate that is 3 to 4 times the selected LPF cutoff, unless a greater rate is useful for subsequent beamforming operations.

Each card has an address programmed with an 8 bit DIP switch allowing as many as 256 cards to be bused. (A more practical limit due to line driving considerations is probably no more than half that). The host computer uses a standard communications (COM) port via an optically isolated interface to communicate with individual cards. This serial link is bused also so that each card responds only to commands preceded with its unique address. The protocol used is similar to the familiar Serial ASCII Instrumentation Loop (SAIL, IEEE 997-1985) format of preceeding commands with "#aa" where "aa" represents a hex address.

3.2.8 Data Transmission

Approximately 75 μs after reception of a sample pulse, the new 2 byte sample is loaded into latches whose outputs reside on the system data bus (Figure 26). At high sampling rates, the controller is processing the previous sample as the new one is being acquired. There is a "RDY" line that is bused such that when all cards have a new sample, it goes to a high level, indicating to the GRA interface in the host that a sample suite is ready to be off-loaded. To read a sample from a card, the host must issue the card's 8 bit address on the system address bus, which enables the data latch outputs for that particular channel. This transaction will be described in detail later.

3.2.9 Power Requirements, Packaging, Interconnections

The GRA requires 4 power supply voltages. Thirty-six channels in 3 chassis consume 5 amps @ +5V, 3 amps @ -5V, 2.5 amps @ +12V, and 2.5 amps @ -12V. This adds up to about 2.8W per channel. The +5 volt supplies all digital devices and the +5V analog requirements of the ADC's. All other analog power is $\pm$12 V because of the input signal swing limitations of the ADC's. Separate digital and analog grounds are run from each chassis of 12 GRA's to the supplies. Power packs were made up of 3 amp +/- 12 volt and 6 amp +/- 5 volt units. Each supply is metered for voltage and current and is liberally cooled. A single power pack can run 3 full chassis of 12 GRA's.

A single 12 channel chassis is a standard 19 inch rack mount, 7 inches high. Since all connections but the analog input to each signal are bused, a printed circuit backplane was designed to accommodate 12 - 100 pin edge connectors and a 50 pin header for a flat cable connection to the rear panel. This is just visible on the left of Figure 42 showing the front view of a chassis. All signals on the backplane have ground runs between them to minimize interference and noise. Particular attention was given to isolation of the analog inputs to minimize 60 Hz contamination. Power supply traces are doubled.

The rear panel connections shown in the photograph of Figure 43 are:

- The 12 isolated BNC inputs at the top are for analog signals. Connections to the card edge connectors are coax.
- The 50 pin blue ribbon connector is the system data/address/control bus. All chassis are connected on the same 50 pin flat cable.
- The power supply connections are made using forked lug crimp connectors on twisted pair, #16 wire. A separate set of power cables from each chassis connects up to 3 to a power pack.
- One chassis in a system must power the optically isolated serial interface from the "+5D" BNC shown. All chassis have the "C" BNC (for communications) bused to the serial interface. The "F" BNC's on all chassis are bused to the sample pulse source. The "A" BNC corresponds to the "DCCAL" input on the GRA cards and is used for DC calibration.

3.3 Software

The 87C51 processor was chosen for the GRA controller not so much for unique characteristics as for previous experience with it in other systems. It is probably one of the 2 best known 8 bit controller types, the second being the 'HC11 family from Motorola and elsewhere.

The code for the GRA function is in native assembly for speed. It was expected that the maximum sampling rate was going to be determined by the rate at which the controller could determine gain and make the offset correction. A core algorithm for determining gain executes in a maximum of 25 μs. Up to 18 μs more is required to make the offset correction, make the new sample available and display status in the form of the "RDY" and gain indicator LED's.

About 3.5k bytes of the available 4k bytes of code space are used. About 25% of that is alloted to the sampling-with-continuous-offset-update and fixed gain modes of operation that have not in fact been used much in practice.

GRA functions are invoked in 2 ways: i) when more than 1 card is on the bus, the *System Level Commands* are usually used, whereby the card address is part of the command, ii) when a single card is used, or when it is desirable to quickly output the same command to all cards on the bus, *Global Commands* can be used, whereby no card is specified in the command, and all cards respond in sequence based on their address. In response to all

system commands, a card will respond with 3 ASCII characters; a dash followed by 2 hex digits representing the card's address.

Serial communications are conducted on an interrupt basis so that no time is wasted poling the serial port for commands while acquisition is in process. Since there are few circumstances when interrupts are disabled, there is little chance that an amplifier will fail to recognize a serial command. The default and maximum baud rate is 4800. When a character arrives via the serial port, the interrupt routine checks for a "#". If received, a command is expected and the card address is read. If it's the correct address, the command is read and executed, otherwise, the command is ignored and the search for "#"is resumed.

The features and operational modes supported by the GRA software are described below. In many cases, there is a one-to-one correspondence between System and Global commands. In all descriptions, "aa" is a card's address and the hex characters "Fn" are for *System commands* when preceeded by a card address and for *Global commands* without an address).

GRA Functions:

- Soft Reset; System code #aaF0, Global code #F0. All functions of the GRA are reset, however the channel address DIP switch is not reread. (The only way to get that to occur is a hard reset with the manual button on each card, or a power-on reset.) The GRA performs the following functions:
  - reset, clear stack
  - blink the green RDY LED, blink the 4 red GAIN LED's (delayed briefly as a function of the card address)
  - recalibrate the 5 ADC's
  - load a default value of 80 Hz into the LPF
  - de-select the HPF
  - set the PA gain to 1
  - set the baud rate to 4800
  - clear diagnostic codes
  - invoke offset calibration
- Enable for Sampling; System code #aaF1, Global code #F1. After reception of this command, a channel will respond to a falling edge on the sample input by taking a sample. Without this command, a card will not take samples. This is normally the last command issued to cards prior to initiation of sampling. All LED's will be out until sampling starts. During sampling, the green RDY LED glows as a function of sample rate. Cards with higher addresses will show a brighter RDY LED because it is on from the time the sample is ready until it is read by the host computer. If the red ERROR LED turns on, it indicates that at least 1 sample was missed. It remains on until another control command is executed.
- Enable Sampling, Update Offset; System code #aaF2, Global code #F2. This function is similar to the above, however the samples are summed continuously to provide

an updated offset value every 64k samples. All LED's on selected channels will be out until sampling starts. Status LED's will then display as described for command "F1". This mode can be invoked for sample rates as high as 2500 Hz from the standpoint of computational overhead. The benefit over the normal sampling mode is that at lower sampling rates, acquisition runs may be prolonged (many hours), and offset may drift. This technique can accommodate that by regularly summing 64k samples, computing the average and using the residual as the offset value. This mode has not been used because of concern that the variability with as few as 64k samples is nearly .5% of the 64k sum however we think that the concept is reasonable if a factor of 10 or more samples is used.

- Set LPF cutoff; System code #aaF3nn, Global code #F3nn. The LPF cutoff (-3dB point) is programmed using this function. The 2 hex digits *nn* set the cutoff to (nn+1)20 Hz. The minimum value is 20 Hz and the maximum is 5120 Hz. Once set, the filter remains at that cutoff until this command is used to change it or a hard or soft reset occurs. The 4 gain LED's will blink in response to the Global code but there will be no visible response to the System code.

- Halt Sampling; System code #aaF4 Global code #F4. After this command is received, the card ignores further transitions on the sample input and commences the offset calibration process. No other parameters are changed....the LPF, PA gain, etc are unchanged. The 4 gain LED's will blink in response to the Global code but there will be no visible response to the System code. Neither the red ERROR LED or the green RDY LED should be on. If the red LED is on, it means that 1 or more samples were missed. If the green LED is on it means that when sampling was halted, the last sample was not taken from the channel (not a problem but this should not normally occur). The ERROR LED is the most important indicator of successful operation.

- Set Preamp Gain; System code #aaF5n, Global code #F5n. The on-board fixed PA has 8 gain settings in binary steps. The gain code is the exponent of 2 that equals the resultant gain. Valid codes are n = 0 through 7 corresponding to linear gains of 1 through 128. The 4 gain LED's will blink in response to the Global code but there will be no visible response to the System code.

- Set Baud Rate; System code #aaF6n, Global code #F6n. As with the PA gain set command above, the baud rate is set according to the hex byte code "n". Valid codes are n = 0 through 4 corresponding to 300, 600, 1200, 2400, 4800 baud. The default rate is 4800. After the rate is changed, the host serial port must also change to continue communications. The 4 gain LED's will blink in response to the Global code but there will be no visible response to the System code.

- Set GRA Gain; System code #aaF7n, Global code #F7n. Normally cards are used in the default autoranging mode. They can also be configured to run in fixed gain mode with one of the 5 available gains selected. The codes 1 through 5 correspond to gains of 1, 8, 64, 512, & 4096 respectively. A code of 0 requests ranged gain. The 4 gain LED's will blink in response to the Global code but there will be no visible response to the System code.

- Set Slew Delay; System code #aaF8n, Global code #F8n. The hex value *n* is the slew delay in number of samples. During auto-ranging, when the level at any of the upper 4 gains is above 82% (upper 3 bits of the word set) that gain cannot be selected. If the level at a gain is not above 82% of full scale, a check is made as to how many samples have occurred since that gain was found to be onscale. This is referred to as the slew delay and defaults to 3 samples. That means that in addition to being below 82% of full scale, a gain must have been on scale for at least the 2 previous samples before it can be selected for the current sample. In other words, gain will be decreased immediately but increased only after a gain range has been onscale for a minimum time related to the sample rate. At a 20kHz sample rate, a delay of 3 means that the output at a given gain range must have been onscale for a minimum of 100 μs. The 4 gain LED's will blink in response to the Global code but there will be no visible response to the System code.

- Disable Channel; System code #aaF9, Global code #F9. This command is used to deselect channels so that they are effectively removed from the bus during data acquisition operations. In this mode, the green RDY LED is constantly on. During acquisition runs, cards that are not used should be left in this condition. Normally this command is issued to all cards followed by the "F1" or "F2" command to enable those that are to be active during subsequent data acquisition.

- Diagnostic Sampling 1; System code #aaFAn, Global code #F9n. These diagnostic operations are used for test purposes to verify basic functions of a GRA. This command with *n=0* allows continuous testing of the controller's interaction with the ADC's by configuring the card for normal sampling but latching a count down hex value starting at 0xffff and proceeding to 0 as sample edges arrive. The same command with *n=1* will cause the card's address to be placed in the output latches after each sample period. The ADC's are setup normally and in fact do sample. The 512X ADC is monitored as usual to know when sampling is complete and its data is read out to enable the next sample.

- Diagnostic Sampling 2; System code #aaFBn, Global code #FBn. For diagnostic purposes to check that offset calibration and sampling of the normal and DCCAL inputs are functional. The following *n* codes are available:

  1. *n=0*, normal offset calibration process is invoked with the outputs of all 5 gain ranges displayed on the screen with the resultant complemented correction factor shown as well.
  2. *n=1*, continuously display the value of all 5 ADC's with the LPF input shorted. This is a means for making the only offset adjustment on the board which is a pot on the AC coupling amp before the amplifier chain. Once this is done during the initial card setup, it will probably no longer be required. No offset correction value is computed or modified during this test.
  3. *n=2*, sample the standard input at an internal rate, which is slow enough to display...only a couple of Hz. The offset corrected values from all 5 ranges are displayed.

4. *n=3*, sample the standard input at an external rate applied to the sample period input. The offset corrected values from all 5 ranges are displayed.
5. *n=4*, sample the DCCAL input and display the resultant value after DC offset correction. The DCCAL input is applied to the amplifier chain DC coupled so it can be used to calibrate the ADC's with DC levels at minimum and maximum values.

- Request Pulse Calibration operations; System code #aaFC, Global code #F9. One of the concerns of a multichannel system is the inability to test with confidence the operation and accuracy of all the cards quickly enough that it can be done routinely in the field. It can be difficult to identify a card that is misbehaving. The intention here is to be able to apply a single "boxcar" pulse of some fixed duration and amplitude, to the amplifier input. Samples are acquired by the host at a selected sample rate. At the host, the spectrum of the impulse would be computed and energy levels compared at specific frequencies with a stored replica of what the response should be at one or more LPF settings. In this way a complete system test can be accomplished in a short time that can be used as a "go-nogo" criterion at any time and be a rigorous test of all sections of the GRA.

  This feature has never been fully implemented, partly because there is no easy way to get the same pulse input to all channels without operator intervention at the rear panel DCCAL input. Thought has been given to committing the DCCAL input to a replica of an accurate portion of the ADC voltage reference. This would only have to be done to one card in each chassis as the DCCAL input is bused.

3.4 Test Data

Three sets of spectral plots are shown to demonstrate the amplitude characteristics of the GRA. They are: 1) noise floor, 2) dynamic range & harmonic distortion, 3) Lowpass filter. The Y-axis on all plots is dB relative to 1 Volt (dBV), un-normalized "per Hertz". The per Hz correction can be had by subtracting 10log(bin-bandwidth). In all cases the FFT size was 512 complex, therefore with a 500 Hz full scale bandwidth, the dBV numbers are essentially per root Hertz. Appropriate figures are cited in each section.

3.4.1 Noise Floor

The same channel was used for all plots and can be considered representative. The input was DC coupled and open (it is terminated on-board with a 33.2K resistor). The sampling parameters are given on each plot. Normally an average of 8 spectral frames is shown. At a PA gain of 1, the input can swing a maximum of ± 10 volts or approximately 7Vrms (+17 dBV). Spectra of the broadband noise floor at PA gain settings of 1 & 16 are shown in Figures 2 & 3. The LPF was set at 80Hz. Note that the effect of the on-board PA is to position the measurement range of the system relative to the noise floor of the LPF, i.e., if input signal levels will never exceed -20 dBV it may improve data quality to apply up to 24 dB gain at the PA.

Gains of 32, 64 and 128 are available but gain beyond 16 are rarely useful as the inband noise floor doesn't decrease significantly beyond about -140dBV. It can be seen that by themselves, the GRA's do not suffer from 60 Hz contamination. The HPF was not included but has no significant contribution to noise compared to the LPF.

3.4.2 Low Pass Filter Response

Sample spectral plots are shown to demonstrate the LPF amplitude response at 3 cutoffs, *4000 Hz* (Figure 4), *260 Hz* (Figure 5), and *80 Hz* (Figure 6). The input for these tests was digitally generated white noise flat to about 20kHz. Again, these plots are not normalized to 1 Hz bandwidth. The phase characteristics of these filters are classical 8 pole Butterworth with nearly linear group delay to about half the cutoff frequency.

3.4.3 Distortion

A series of tests were run to demonstrate the effect of gain ranging on harmonic distortion as a function of sampling rate, signal level, and signal frequency. The HPF was not connected for these tests. A representative selection of the results are shown. The test signals were tones from a Krohn-Hite model 4400A, specified to have harmonic distortion levels of -100 dB so it is assumed that the plots show the cumulative effects of the GRA signal conditioning. The signals were acquired with a test program using the same routines as the acquisition system discussed later.

As signal amplitude and the ratio of sample rate to signal frequency increases, samples are acquired from more gain ranges. This occurs because there is a greater opportunity for gain increases as a signal passes through zero amplitude. The slew delay for all tests was 3. It can be argued that a greater slew delay could make distortion due to ranging a non-issue. What is shown is the case where very high amplitude tones, low in frequency relative to sample rate, cause maximal gain changes, and hence worst case distortion levels. Similar conditions are not often encountered in real data.

In Figures 7 through 13, a 100 Hz tone is the input signal at levels of approximately 7 Vrms (maximum input signal) down to -60 dBV in 20 dB steps. The LPF is at 260 Hz, the sample rate is 10kHz and the PA gain is set to 1,16 and 128 as labeled. The LPF is specified to have $\leq$ .03% distortion at 3.5 Vrms. At the maximum signal level, the harmonic components observed beyond the filter cutoff of 260 Hz are not a function of the ranging amplification as they are observed in the fixed gain example of Figure 21. Figure 8 at 100 Hz and 0 dBV, shows the 2nd harmonic about -68dB with ranging and disappears at fixed gain shown in Figure 22. As the signal level decreases, higher gain ranges are used. At the higher signal levels, it is possible that the 36dB gain range is used but usually only the 0 and 18 dB stages are sampled. It is apparent in Figures 12 & 13 that there is little benefit to PA gains beyond 16 since the passband noise floor at 128 is only a few dB lower than at 16. Increasing PA gain beyond 32 simply decreases the measurement range of the amplifier.

Figures 14 through 20 are similar but the signal is at 1 kHz and the LPF is set at 3200 Hz. At 7 Vrms, the highest distortion component is about -64 dB from input. At these high signal levels, the LPF is responsible for the other components that don't appear to

be harmonically related. The plot looks virtually the same at a fixed gain of 1, not shown because the gain at such high signal levels usually remains at unity. Again, there is little difference in the passband between PA gains of 128 and 16.

3.4.4 Crosstalk

Figures 23 and 24 show the effect of crosstalk on a card with an open input adjacent to, and some distance away from a channel with an input at maximum level. There is about a 20 dB peak at the signal frequency in the adjacent channel but it is about 110 dB down from the input on the channel with signal and somewhat smaller on the more distant channel.

4 Acquisition System

In this section, the acquisition system hardware, software, data storage and directory formats are described. The objective of this system design was to be able to acquire and store data at relatively high continuous rates using an inexpensive PC. We wanted to be able to acquire data limited only by the continuous storage bandwidth of the storage device, allowing upgrades as faster devices became available. To permit continuous recording to an archivable medium, it had to be removable and high density.

The system currently has 40 of the GRA channels just discussed, a PC/AT, Industry Standard Architecture (ISA) bus computer, GRA interface and one or more Write-Once Optical Disk (WORM) drives. The system configured as shown in Figure 25 has been in the field and successfully recorded data on 2 occasions; the CEAREX experiment in 1989 and the Heard Island Feasibility Experiment in 1991. The acquisition software was upgraded in 1990 to incorporate realtime display-after-write features.

4.1 Storage Medium

The optical disks are Optimem 1000M drives, using 12 inch, 2 - sided platters storing 1.0 or 1.2 gigabytes (GB, $1 * 10^9$ bytes) per side. The interface is a single ended version of the Small Computer System Interface (SCSI), supported by a $250 host adapter in the PC. The drives are now about 5 years old but are still among the fastest available, capable of storing data at 420 Kbytes/sec *continuously*. Though the newer Optimem 4000 drive with 2.0 GB per side doesn't offer the highest density (other WORM's can now store up to 3.5 GB per side), it offers about a 50% greater *continuous* storage rate. The drives we are using cost about $12k and the newer models are about $16k. The media cost can often be the decisive factor in storage method selection. The Optimem disks cost $500 to $700 which is at least 50% greater than the higher density media used by the slower 12" Sony drives.

The Exabyte 8mm tape drive could be used in place of the optical disk drives. The media cost is very low and the new 8mm units have similar storage bandwidth however the random accessibility of the data is very much slower.

4.2 Computer

The ISA bus computer is an inexpensive 286 or 386 machine with a standard 8 MHz bus clock and 8 Mbytes of memory. The GRA controller was designed to use the host direct memory access (DMA) capability which can access extended memory. Many of the cloned AT machines use chip sets that allow the DMA "SCLK" to be increased from 4 to 8 MHZ. At this rate a 16 bit DMA transfer is accomplished in .5 μs, i.e. up to 4 MB/s transfer rate across the bus to/from 16 megabyte memory space. This, with a SCSI host adapter capable of 2 MB/s transfers to the optical disk makes it possible to achieve 1 MB/s net acquisition bandwidth.

The host communicates with the GRA's directly for configuration purposes via a standard COM port and an optically isolated link. The rationale behind the isolation is the minimization of noise contamination of the analog signals by the host. It is possible that this precaution is unnecessary, which would simplify the serial connection.

4.3 GRA Interface

The GRA data/address/control bus, Figure 26, is connected to the GRA interface, a 16 bit ISA bus card designed specifically for this application. A functional diagram is shown in Figure 28 and a photograph of the card is given in Figure 41. The ISA bus is reproduced in Figure 29 and the connections to the acquisition parameter panel are shown in Figure 27. Figure 30 is a synopsis of pinouts from the GRA to the interface, including connections suitable for use with an earlier model GRA. The interface consists of the following sections shown on the interface schematic in Figure 31.

- A sample buffer implemented in a 1k by 18 bit FIFO
- A sequencer, implemented in a 1k by 18 bit FIFO
- Timing and sequencer control implemented in an ALTERA EP1800 PLD
- IRIG-B time code reader and realtime clock synchronizer
- Acquisition parameter generators and realtime clock implemented in 82C54 counter-timers

The GRA controller is a combination of a first-in first-out (FIFO) based state machine and software that allows the runtime configuration of up to 12 I/O lines to control a data source, normally but not limited to a bank of GRA's. Eight of these lines comprise the GRA address bus that selects a channel for data output. Four lines are used for internal control and 4 are unassigned. The assertion of a high level on the RDY line initiates a sequencer cycle that steps through each active GRA address and clocks 2 byte data values into a 2nd 1k X 18 FIFO that is used as a data buffer between the GRA's and the DMA transfer to host memory. The timing for this is shown in Figures 33 & 34 for 1 channel and "n" channels respectively. The sequencer is clocked at 4 Mhz, allowing 250ns for each state. Each channel is interrogated for its data value in 4 cycles for a maximum transfer rate from

GRA's to interface of nearly 2 MB/s. The coding created by the acquisition program and loaded into the sequencer is shown in Appendix A.

A bank of 3 - 82C54's are programmed at the start of an acquisition run to provide a variety of synchronized parameters. The available functions are:

- A sample period generator with 1 μs resolution and 64k μs maximum period with software enable
- A 2nd sample period generator with external input and 64k period maximum with software enable
- "Master" rate with millisecond or second resolution and 64k ms or sec maximum period with software enable
- A "Delay Window from Master" with millisecond or second resolution, and 64k ms or sec maximum period with software enable
- External "Master" input, rising or falling edge
- 1Hz and 1 kHz outputs
- A realtime clock with 1μs resolution
- An IRIG-B synchronizing capability allows quick reading of the timecode to set the realtime clock and sync the system to within about 50 μs of the IRIG source.
- All outputs are buffered and can be programmed for falling or rising leading edge.
- External edge sync capability

IRIG-B timecode is used establish realtime synchronization with millisecond or better accuracy. Compared to the hardware needed to read many BCD digits from an external clock it is much simpler to read IRIG-B and much more likely to be available since it can be obtained from many sources including satellite based systems such as GOES. A software routine was written to read the timecode using the circuit in Figure 32. Synchronization is easily achieved over a wide range of timecode amplitude. Accuracy of the synchronizing routine can be checked and "tweaked" by comparing the timing of 1 Hz clocks between an IRIG source and the acquisition system time base. When synchronized, the leading edge of the 1 ms width pulse at the 1 Hz output should be lined up with the leading edge of the 1 Hz output from the synchronizing source, as well as the rising edge of the GRA interface 1 kHz output.

Typically, a rhubidium timebase is used to assure stability. A UPS (battery backed power supply) is used to run the timebase and the source of the IRIG standard if retention of absolute time sync is critical.

The Altera EP1800 PLD was used to eliminate much of the "glue" logic needed to implement many of the control functions. This 48 cell part replaced about 30 devices and allowed easy design modification, important to a unique system. Without doubt there is a cost in time and effort to learn use of the PLD but in the long run it was clearly worthwhile. Figures 35, 36, & 37 represent the functional internals of the part as programmed.

Synchronous operation is the preferred mode for these devices and it is difficult to achieve timing relationships relying on device propagation delays as one can do with discrete gates. In this design there are 2 unused cells and 3 partially commited. The real advantage is that this controller board could be printed (the present unit is only wire-wrapped) yet remain flexible because even the hardware is somewhat programmable. Figures 35 and 36 are primarily devoted to sequencer, DMA reload and realtime control. The circuitry in Figure 37 in related to acquisition parameter control.

4.4 Acquisition Software

The acquisition software is entirely in C, using Borland's Turbo C, and consists of a main program, and 3 sets of routines related to acquisition functions, SCSI transaction functions and graphics functions for realtime displays. There are about 2000 lines of code. In addition a number of utilities have been written for test and diagnostic purposes and for data quality verification. The challenges of the acquisition task were:

1. conduct the data acquisition and recording in a pseudo backround mode since it's beyond the direct response capability of the processor and DOS
2. maintain precise time stamping of and checking for incomplete data packets
3. under most conditions, permit some modest display of data for quality assurance.

The software configurable aspects of the GRA controller are key to satisfying these requirements.

An ASCII file that is the template for an acquisition run is edited beforehand to contain all necessary information about all GRA channels to be used. Included is information about sample rate, filtering, sensors, the number of channels connected and which are to be used during the pending recording session. The program reads this file, displays portions on the screen for verification, configures the GRA's, programs the acquisition parameters and the sequencer on the GRA controller, synchronizes to the IRIG timecode if requested and awaits a keyboard hit to start sampling. It can be set up so that everything is done by invoking a single short batch file. Figure 38 is an abbreviated version of this template. The acquisition program keys on the colons to read parameters.

The host DMA and interrupts are used to handle the time critical functions of the process. DMA addressing includes use of a page register that permits access to the extended memory region beyond 1 MB. One DMA channel is used by the SCSI host adapter for transferring data from memory to disk and one is used by the GRA controller for writing data to memory. To have sufficient compliance with SCSI transfers, multiple buffers are setup in memory with arbitrarily large size. An important motivation for large buffer space is that the Optimem drives may execute an auto-focus procedure at any time after an hour's operation, that takes up to 1 second during which no SCSI transfers take place. Buffers can be put anywhere in memory but usually larger is better and 4 to 6 - 1 megabyte (MB) chunks are used. The DMA facility of the PC/AT is constrained to a maximum of 64k words per transfer, 128 kilobytes, (KB) so the DMA registers must be reloaded 8 times to fill a 1 MB buffer. To accomplish this while minimizing host interaction, an interrupt

routine is executed when the terminal count (T/C) line on the AT bus goes active. This routine reloads the DMA registers with predetermined pointers and updates pointers to the next sub-buffer. When a "last" sub-buffer is enabled, this interrupt routine sets a flipflop so that at the next T/C, a second interrupt routine reads the realtime clock to get the time to the μs of the first sample of the next 1 MB buffer.

The 1 MB buffers are filled circularly. The foreground activity of the program is to monitor buffer changes and initiate buffer writes, again via DMA, to the optical disk. At each buffer write, status information is written to the screen as to record number, start time of buffer, which buffer was written and which is being filled. The elasticity of the FIFO which buffers data from the GRA's relaxes the timing requirements of the interrupt driven routines. Transfers to memory from the FIFO occur whenever it is $\geq$ half full. This arrangement was accomplished without resorting to timing-critical software, no assembly language, and has worked flawlessly to date.

For data recording well below maximum rates, the acquisition program can be used in a graphics mode that allows 1 channel at a time to be extracted from the last record written to the optical disk and a time series segment or a spectral average displayed on the screen. During the Heard Island experiment a simple delay & sum beam was formed and spectra displayed using data from a vertical array. Because of the large amount of buffering available in extended memory space, these displays were achieved with data rates as high as 320 KB/sec. At this rate however display can only occur about once every minute since time msut be allowed for buffer write operations to "catch up".

4.5 Optical Disk Storage Details

An earlier WHOI technical report #WHOI-87-49, described the initial application of the Optimem disk drives to our data acquisition efforts. The formats used to store data on the disk and the directory structures developed were discussed. They are *not compatible* with any file system and therefore must be read *raw* for analysis. Essentially, those methods continue to be used with, however, a few important but compatible changes which will be noted.

4.5.1 Optical Disk Header

Each optical disk starts and ends with a disk header that is one sector long. There is normally a disk header sector at the first logical block (LBA 0) and the last logical block, (LBA 999999 for 1.0 GB per side disks and LBA 1172499 for 1.2 GB per side disks). The "C" structure of the optical *Disk Header* is shown below. Note that "longs" are 4 byte integers. A sample disk header is printed out in Appendix C.

```
struct disk_header
{
  unsigned char  dhkey[4];      /* disk header key, "ODHD" */
  unsigned char  sn[16];        /* platter S/N, 15 chars, leading */
                                /* zeroes, terminated with null */
```

```
  unsigned short dhtime[4];    /* date/time header was written */
  long           chblk;        /* 999999 (1172499), compact area */
  long           dhblk;        /* normally 0 for file area */
  long           badones;      /* # non-blank sectors originally */
  long           badptr[244];  /* long pointers to non-blank LBA's */
  long           dhcont;       /* continuation ptr or zero if none */
  unsigned char  dhkey1[4];    /* repeat of disk header key */
};
```

4.5.2 Optical Disk Directory

Two copies of file directories are available:

1. The "compact" directory is stored backwards sequentially starting at the last LBA, i.e. at the location of the 2nd disk header. It is a series of directory entries, each one sector long, with one entry per data file. Use of the compact directory is preferred since a listing of all files on the disk will be found in one place, i.e. the end of the disk. On a 1.0 GB/side disk, LBA 999999 would contain a disk header sector, LBA 999998 would contain the directory entry of the first file written, LBA 999997 for the second file, and so on.

2. Separate directory entries, each 1 sector long and identical to the entries in the compact area, are found preceding each file on the disk. This is referred to as the "dispersed" directory.

Information about the size of an entire data file is not contained in the record headers. This, along with information about the file's address, is found in the corresponding directory entry of the file. The following "C" language structures describe the information held in a *Directory Entry* for an optical disk file. A sample directory entry is printed out in Appendix D.

```
struct dir_pair
{
  long           ptr;          /* pointer to file segment starting */
                               /* LBA, doesn't include dir entries */
  long           blks;         /* # blocks in file segment */
};

struct dir_entry
{
  unsigned char  dekey[4];     /* directory entry key code, "ODIR" */
  unsigned char  fname[16];    /* file name <=15 chars, ending null */
  unsigned short detime[4];    /* date of entry */
  long           clba;         /* this entry's LBA in comp dir area */
  long           dlba;         /* this entry's LBA in disp dir area */
  long           bytes;        /* total # bytes in this file */
```

```
  struct dir_pair  dp[122];     /* pointer/length pairs */
  long             decont;      /* continuation ptr or zero if none */
  unsigned char    dekeyl[4];   /* repeat of key code */
};
```

4.5.3 Data Files

The standard procedure is to write data starting at the beginning of a disk, while writing directories backward from the end. Each directory entry is one sector long. Typically two types of files are written: *.DAT files which hold the data, and *.HDR files, which are the ASCII template files mentioned earlier that contain acquisition parameter information pertaining to the corresponding *.DAT files (see Figure 38). The *.HDR files are independent files that have two sets of directory entries as do data files.

A data file is divided into records which have *NO STANDARD LENGTH*! The record length will be constant, however, throughout any given data file. A data file is a contiguous sequence of records, each record beginning with a sector containing a record header,in which the record size, number of chans, etc. is identified. Information in record headers except for record number and the time tag will be the same throughout a file. Following each record header sector is a number of sectors containing multiplexed data strung out in this manner: chan 1 value, chan 2 value, ..., chan N value, chan 1 value, chan 2 value, ...etc. A previous system de-multiplexed data records prior to storage but had very much reduced storage bandwidth.

Data continue to be stored as *unsigned short int* (2 bytes), with the lower byte occuring first followed by the upper byte. Often, the bytes must be flipped when being read depending on the storage format of the processing machine used. The bits are ground true, i.e an active bit is a "zero" or low level. The 16 bit sample consists of a 13 bit, 2's complement *mantissa* (M11 is msb), in the low part of the word with the 3 gain bits in the upper part, (G2 is msb). The sign bit is in the 12th bit position. Bits 0 through 7 are the low byte and bits 8 through 15 are the high byte of the stored sample. A raw data sample, the first 1k bytes in a file is printed in Appendix F.

```
Bit  15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0
     G2  G1  G0  S   M11 M10 M9 M8 M7 M6 M5 M4 M3 M2 M1 M0
     {  GAIN  }{+/-}{              MANTISSA              }
```

Appendix B offers a routine that has been used to normalize raw data blocks to volts at the output of a sensor. Any fixed gains applied to the signal including the GRA PA gain can be applied to the variable *pag*. This routine does not handle byte transposition just mentioned.

There is an equal number of values for all channels in one record. After the last sector in a record (a sector is 1024 bytes on the Optimem disk), the following sector will contain the next record header, followed by more data. In this way, all the data for one file occupies a contiguous area on the disk. [1] Time to the μs of the first sample in any record and the

[1] The WHOI report mentioned above talks about a provision made for dividing up data files into segments

record number are recorded in the record header as shown in the "C structure" used to define the 1024 byte *Data Record Header* given here. A sample record header is printed out in Appendix E.

```
struct data_rec_hdr
{
  unsigned char  rhkey[4];      /* header key, "DATA" */
  unsigned char  proj[16];      /* project name, ascii */
  unsigned char  extype[32];    /* exp type, ascii */
  unsigned short exp;           /* exp number */
  unsigned short date[2];       /* ODAS date...(year, Jday) */
  unsigned short time[2];       /* ODAS time..(minutes, ms) */
  unsigned short ch;            /*  # channels */
  unsigned short bkch;          /* # blocks per demuxed channel */
                                /* if zero, data is not demuxed */
  long           npts;          /* # sample periods */
  float          rhfs;          /* sample rate in Hz */
  unsigned short rlen;          /* record length in blks, includes */
                                /* sector used for record header */
  unsigned short rec;           /* number of record that follows */
  char           rhlat[16];     /* lat, ascii DDD MM SS.T  N or E */
  char           rhlng[16];     /* long, ascii DDD MM SS.T E or W */
  unsigned short lpf[256];      /* LPF setting (Hz) for up to 256 ch */
  short          slew_delay;    /* slew delay...GRA parameter */
  unsigned short microsec;      /* microseconds, <1000 */
  unsigned short sample_mode;   /* 0 = normal, 1 = offset updated */
  unsigned short preamp_gain;   /* linear gain other than ranged */
  unsigned short sample_period;  /* sample period in microsec */
  unsigned short buffer_num;     /* buffer number this record */
  long           rectime;       /* record time in microsec */
  unsigned char  other[382];    /* space left in record header */
                                /* possibly used for sensor locs */
  unsigned char  rhkey1[4];     /* end of rec header key "DATA" */
};
```

In fact there is a constant offset between the time recorded and the actual time of the first sample in a record. The actual time is given by the following equation where "DIFFERENCE" is in seconds.

```
                    FIFO_SIZE = 1024
DIFFERENCE = (FIFO_SIZE/( #ch*sample_rate*2 ))
   ACTUAL TIME = REPORTED TIME - DIFFERENCE
  If FIFO_SIZE/(2*#ch) is non-integer, round up
```

occupying different contiguous areas on the disk. There has never been the need to implement this.

5 Final Comments

We have chosen to use write-once optical disks for data storage for the high recording density, removability of media, standard interface (SCSI), and fast random accessibility. For large amounts of data, an obvious second choice is 4mm or 8mm digital tape. The Exabyte 8500 drive is suited to the data acquisition described here. It has features that make it more effective than it's predecessor, the model 8200. In addition to a 5 GB, uncompressed capacity, it can be configured to write without verification to assure a high, near maximum continuous writing rate (500 KB/sec). It can also be configured to allow power turn-on without rewinding, an important feature for low power applications. The slow random access of the tape can be a significant compromise though when it is time to process data. The low cost of the tape medium compared to optical disks (greater by a factor of 10 to 100 on a cost per unit of storage basis), can be a compelling tradeoff when very large data sets are involved. As for data archiving issues, a case can be made for either medium based on longevity and the evolution of hardware for playback. In many cases, the demise of the record/playback machinery rather than the medium is the determinant of longevity.

The recent introduction of 24 bit sigma-delta analog-to-digital converters by at least one US manufacturer suggests that an auto-ranging amplifier will soon be unnecessary, at least for low bandwidth applications. Crystal Semiconductor is offering 2 versions of a 24 bit ADC. One is a nearly complete 2 chip set with programmable bandwidth to 1500 Hz at a sample rate of 4kHz. In addition to the true 20 bit dynamic range, anti-alias filtering requirements are very much relaxed as bandlimiting is done digitally with very nice group delay characteristics. With this part similar functionality to what has been described here would be possible with very much reduced size and power requirements.

6 Acknowledgments

The technical developments described in this document were supported by the Office of Naval Research, Arctic Programs, Code 1125AR. At Woods Hole Oceanographic Institution, the work was done under grant #N0014-81-C-0161.

7 Figures

8 Appendices

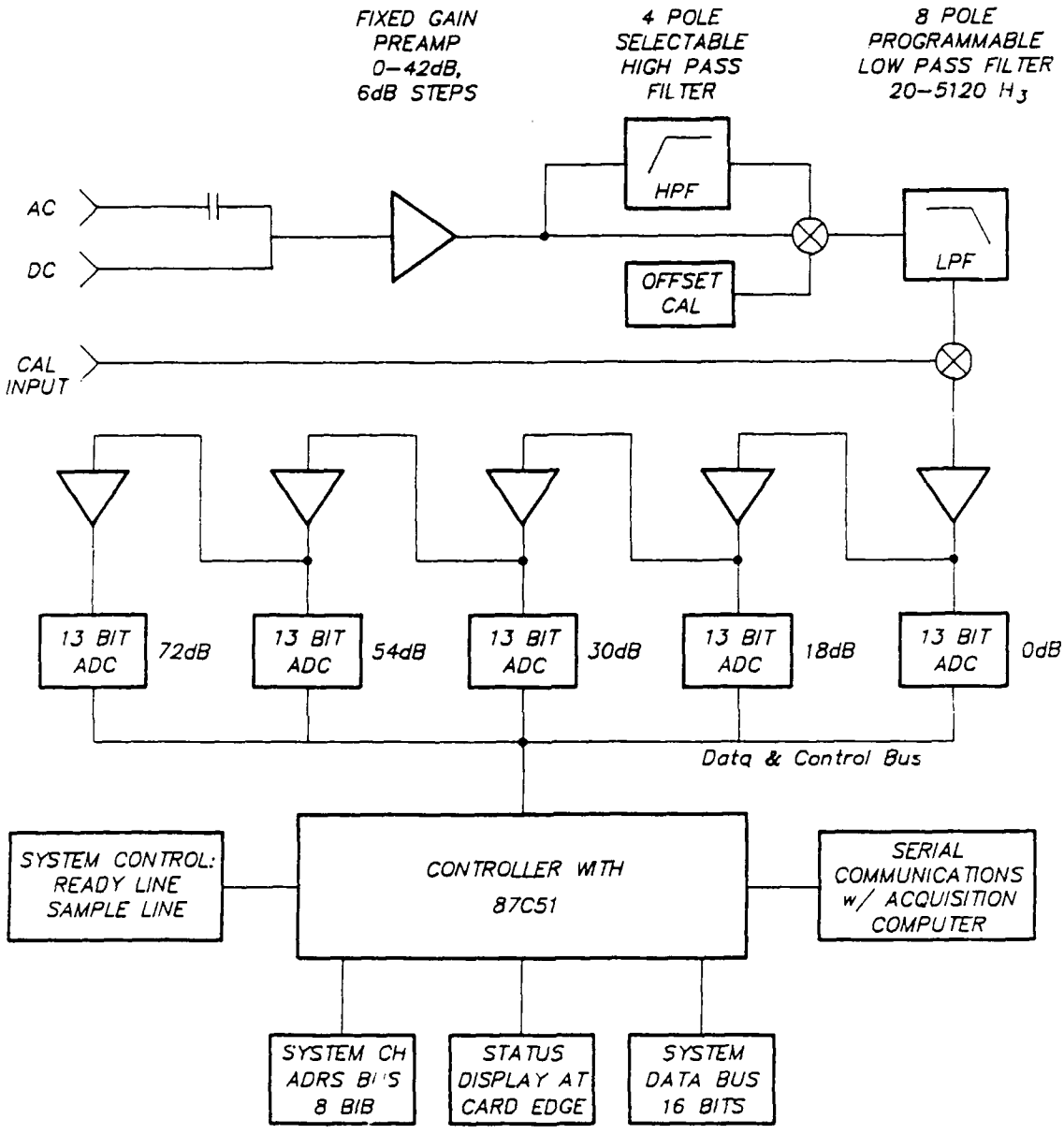


Figure 1. Gain Ranging Amplifier Functional Diagram

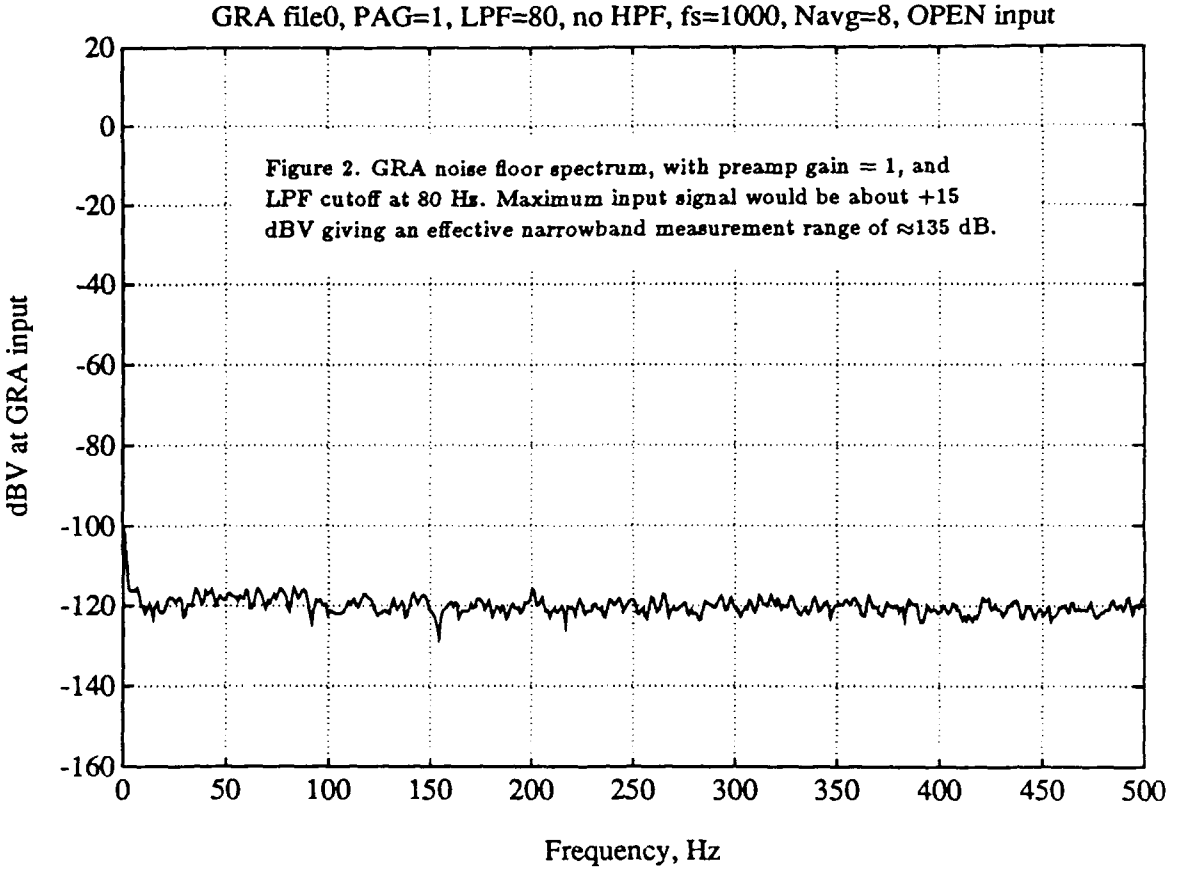


Figure 2. GRA noise floor spectrum, with preamp gain = 1, and LPF cutoff at 80 Hz. Maximum input signal would be about +15 dBV giving an effective narrowband measurement range of ≈135 dB.

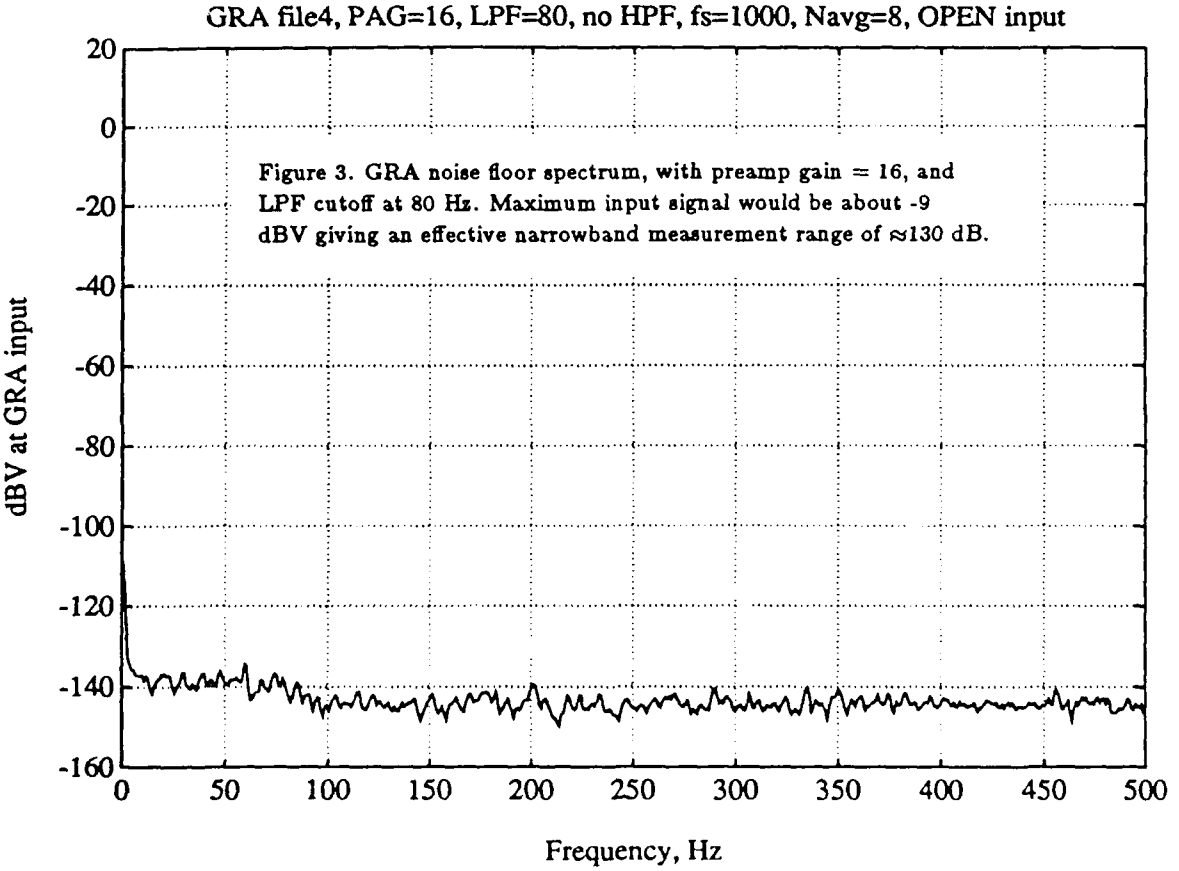


Figure 3. GRA noise floor spectrum, with preamp gain = 16, and LPF cutoff at 80 Hz. Maximum input signal would be about -9 dBV giving an effective narrowband measurement range of ≈130 dB.

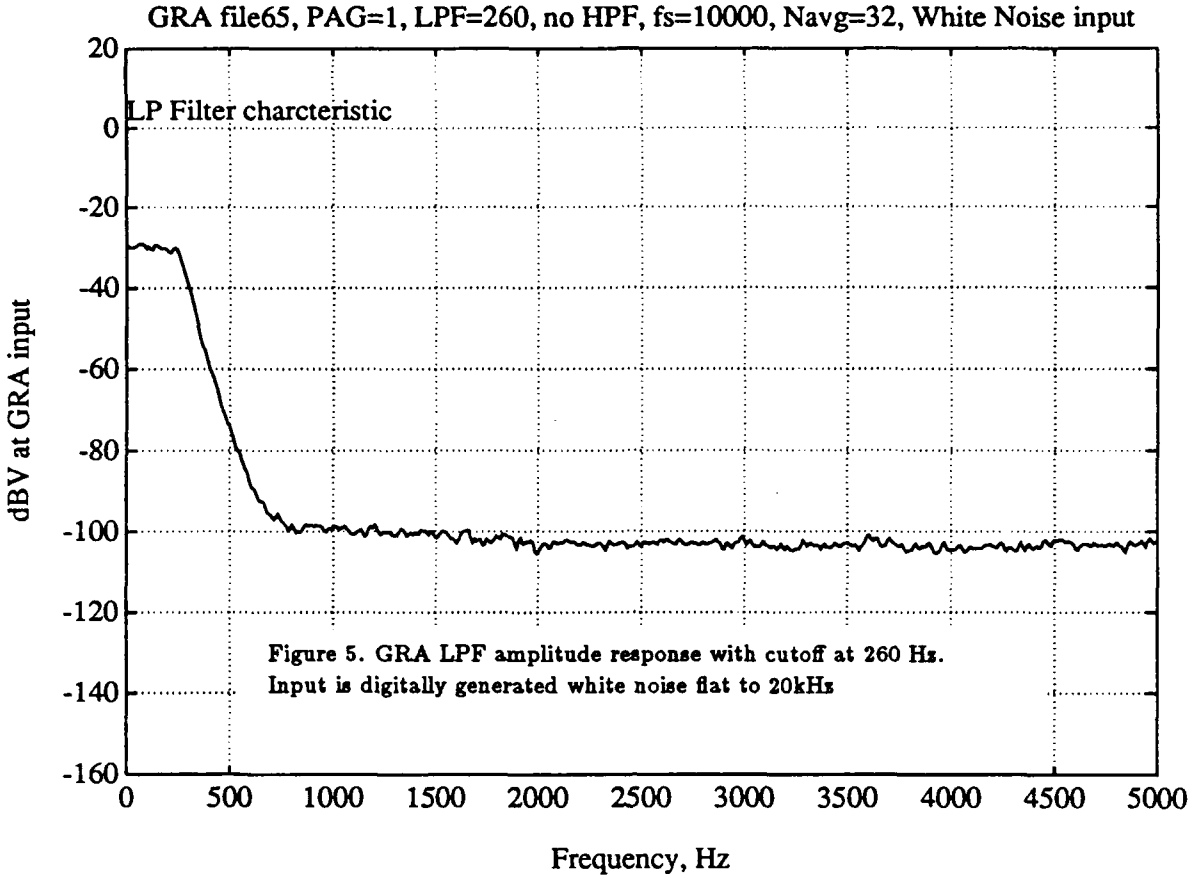


Figure 5. GRA LPF amplitude response with cutoff at 260 Hz. Input is digitally generated white noise flat to 20kHz

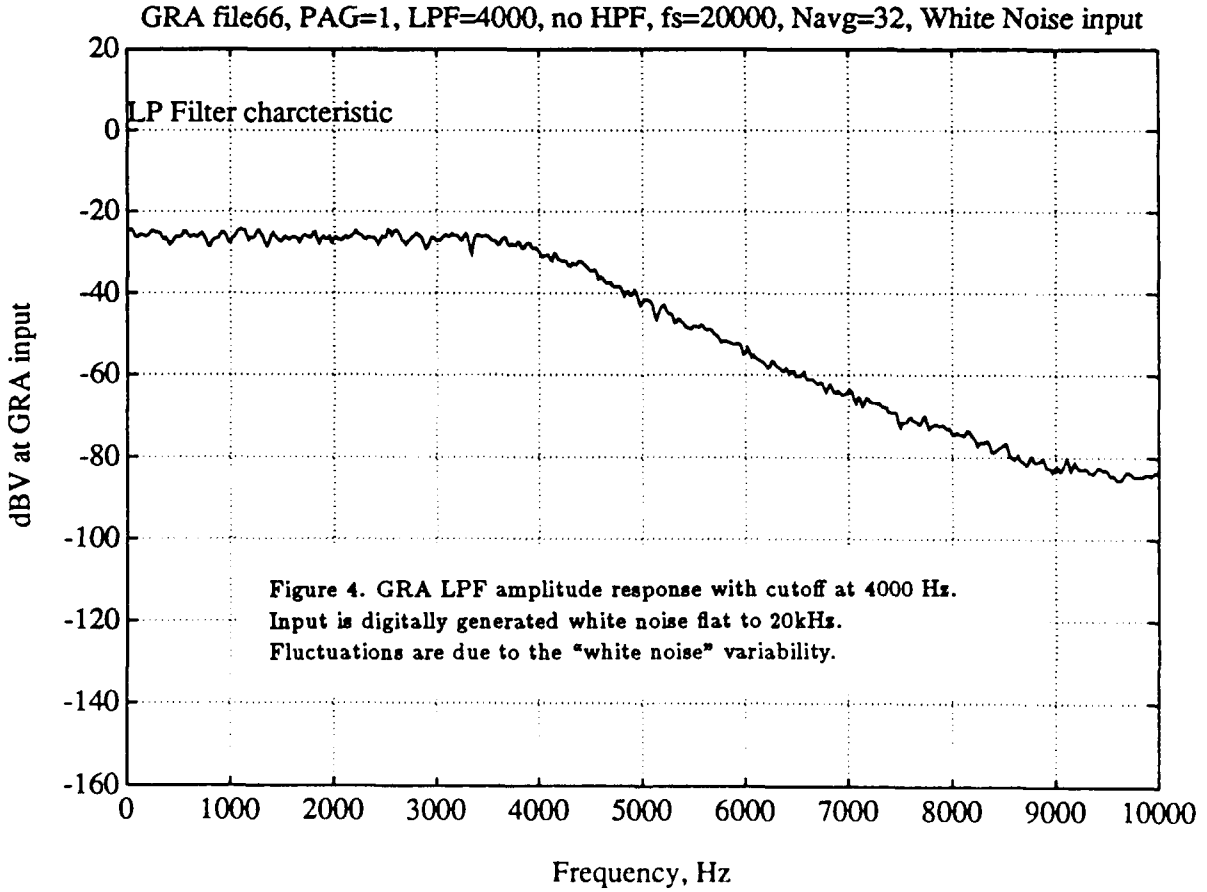


Figure 4. GRA LPF amplitude response with cutoff at 4000 Hz. Input is digitally generated white noise flat to 20kHz. Fluctuations are due to the "white noise" variability.

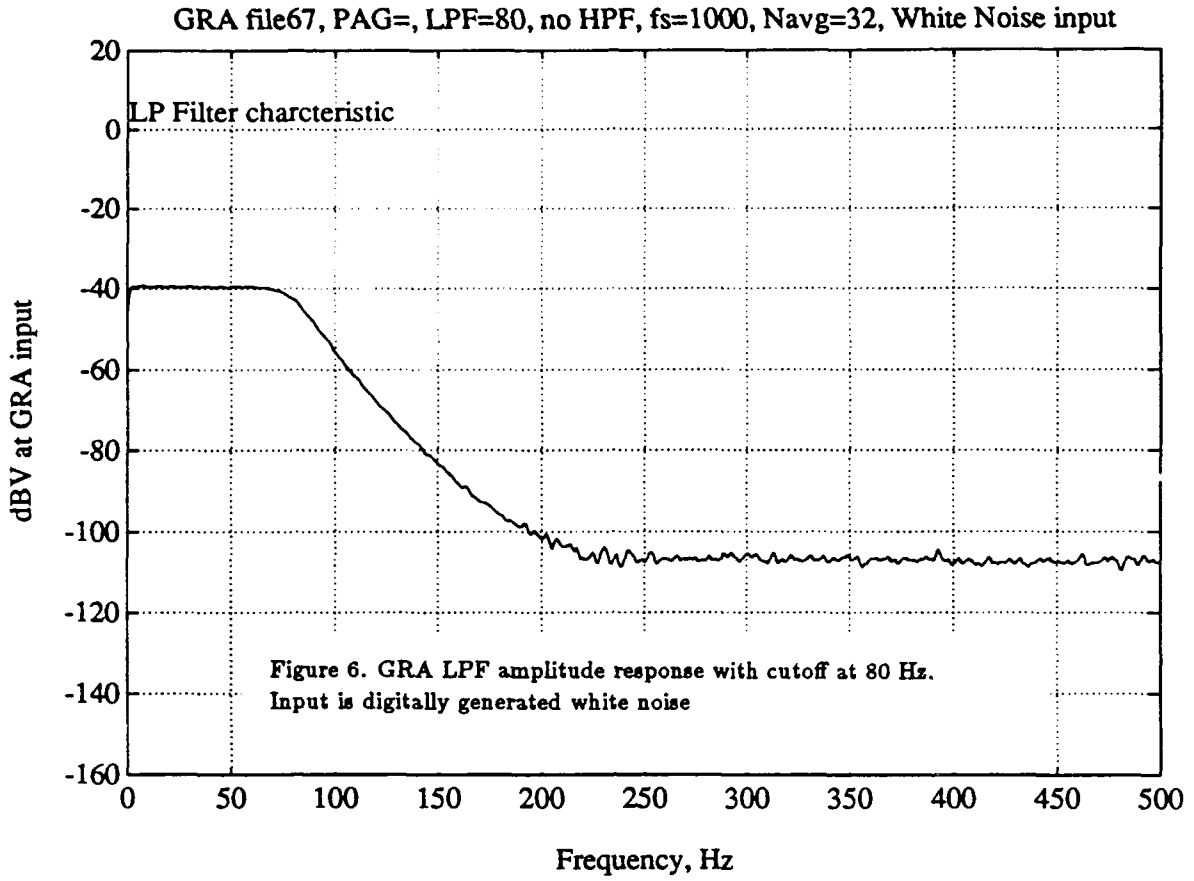


Figure 6. GRA LPF amplitude response with cutoff at 80 Hz. Input is digitally generated white noise

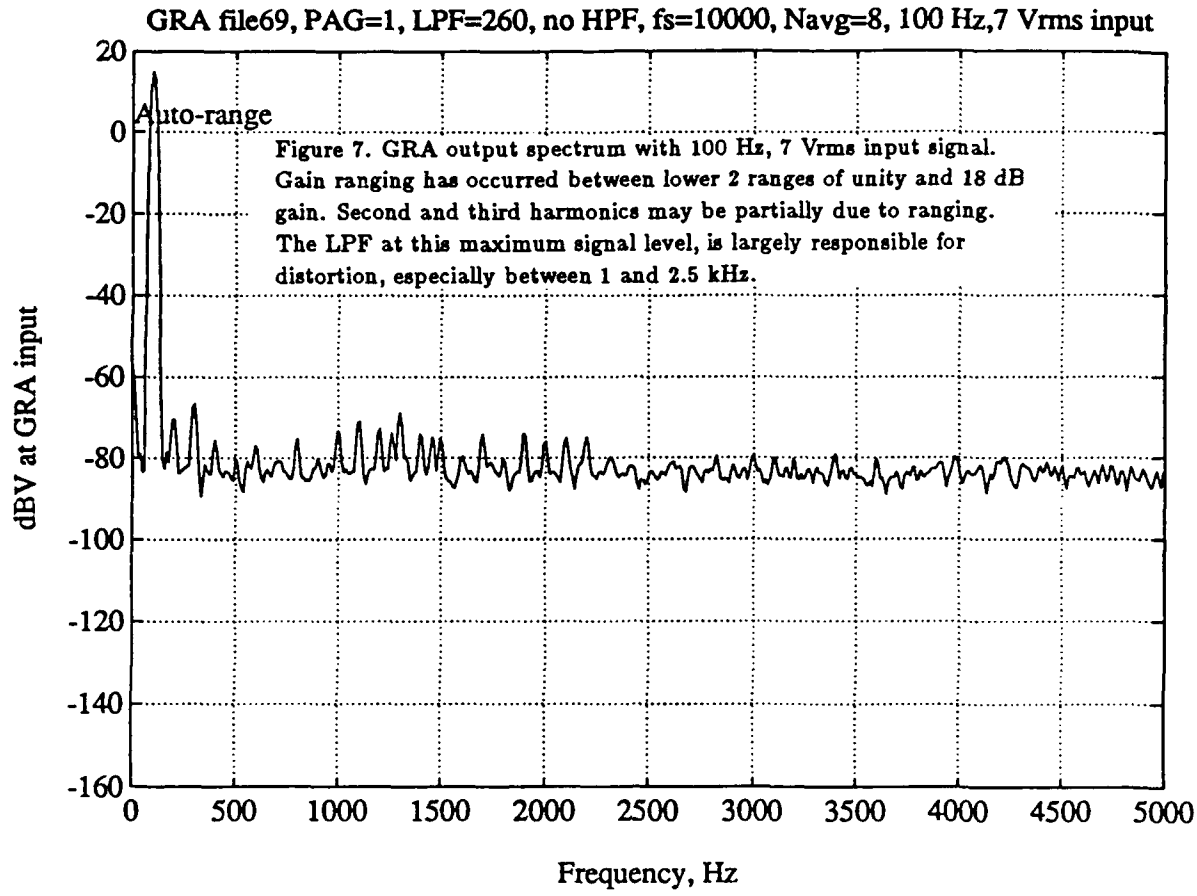


Figure 7. GRA output spectrum with 100 Hz, 7 Vrms input signal. Gain ranging has occurred between lower 2 ranges of unity and 18 dB gain. Second and third harmonics may be partially due to ranging. The LPF at this maximum signal level, is largely responsible for distortion, especially between 1 and 2.5 kHz.

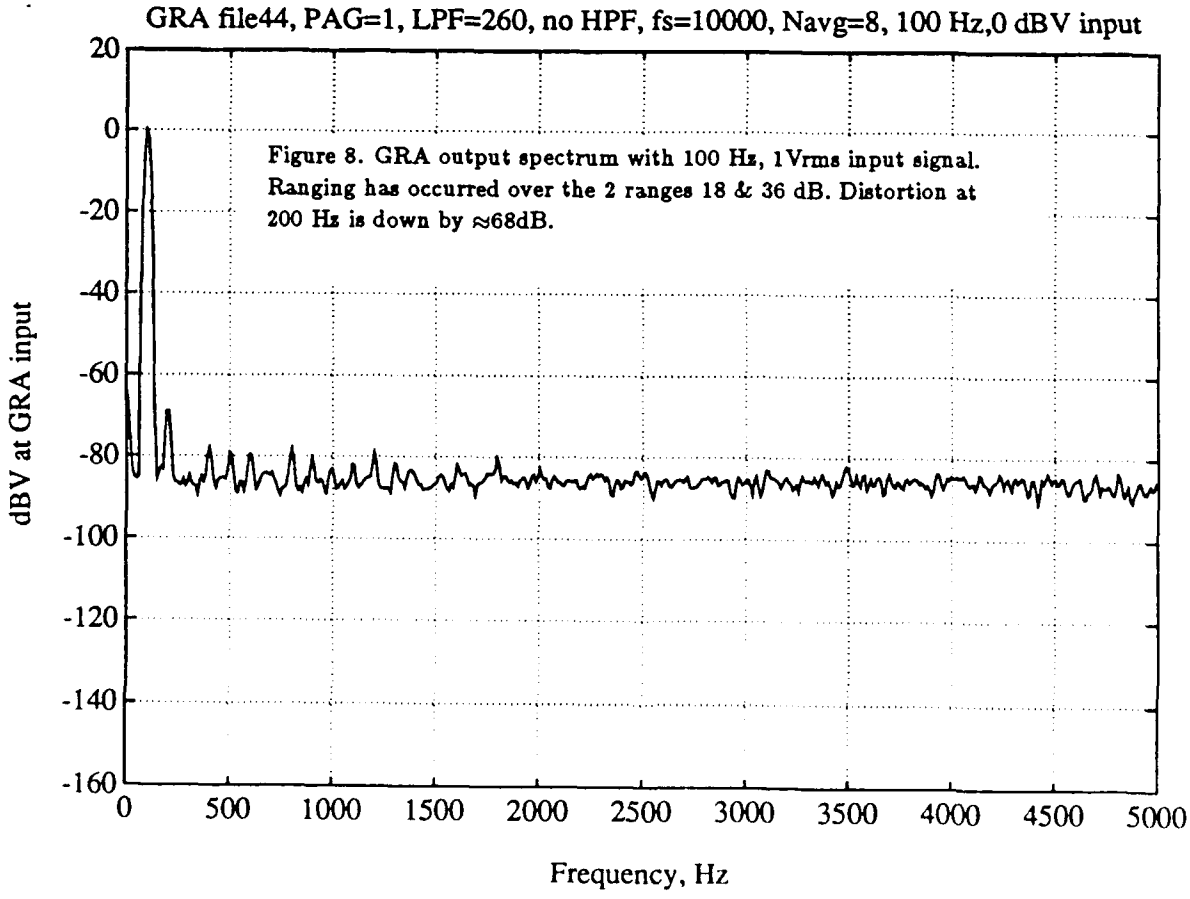


Figure 8. GRA output spectrum with 100 Hz, 1Vrms input signal. Ranging has occurred over the 2 ranges 18 & 36 dB. Distortion at 200 Hz is down by ≈68dB.

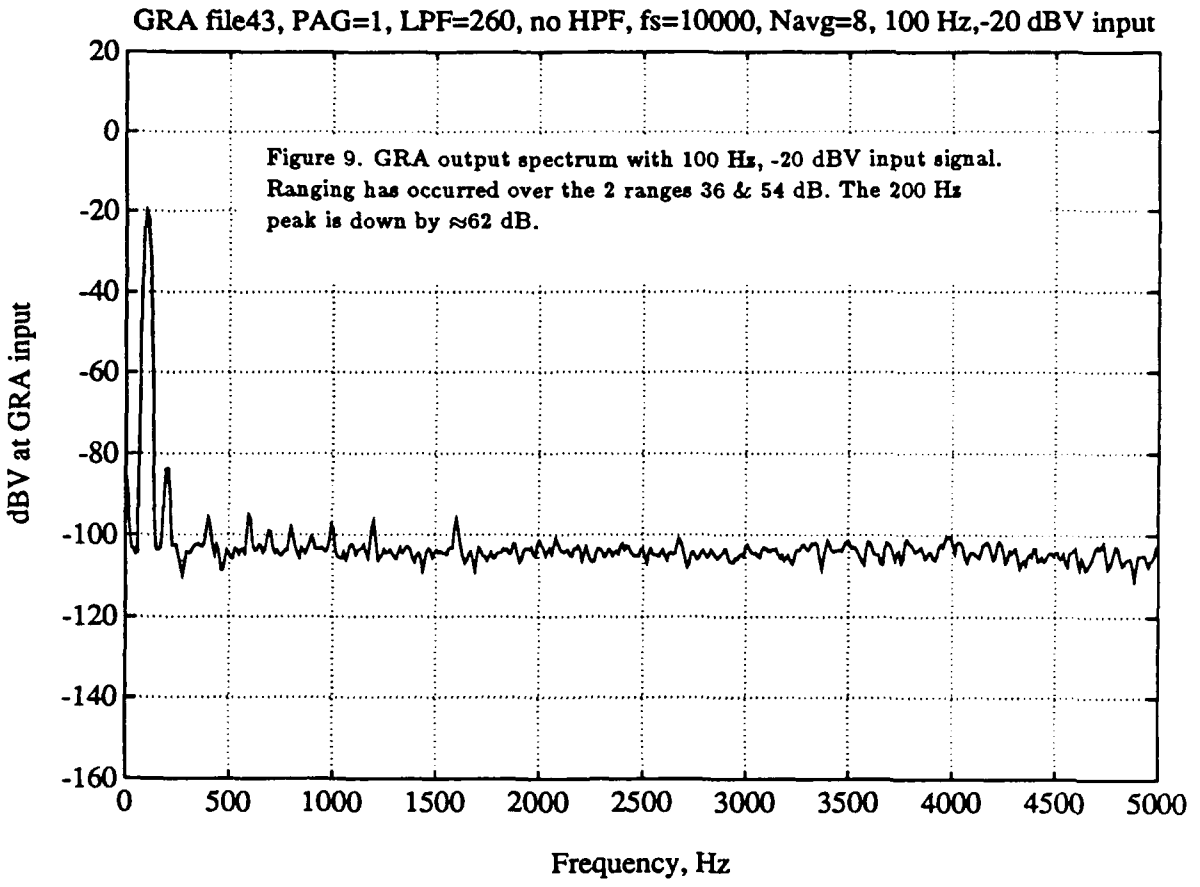


Figure 9. GRA output spectrum with 100 Hz, -20 dBV input signal. Ranging has occurred over the 2 ranges 36 & 54 dB. The 200 Hz peak is down by ≈62 dB.

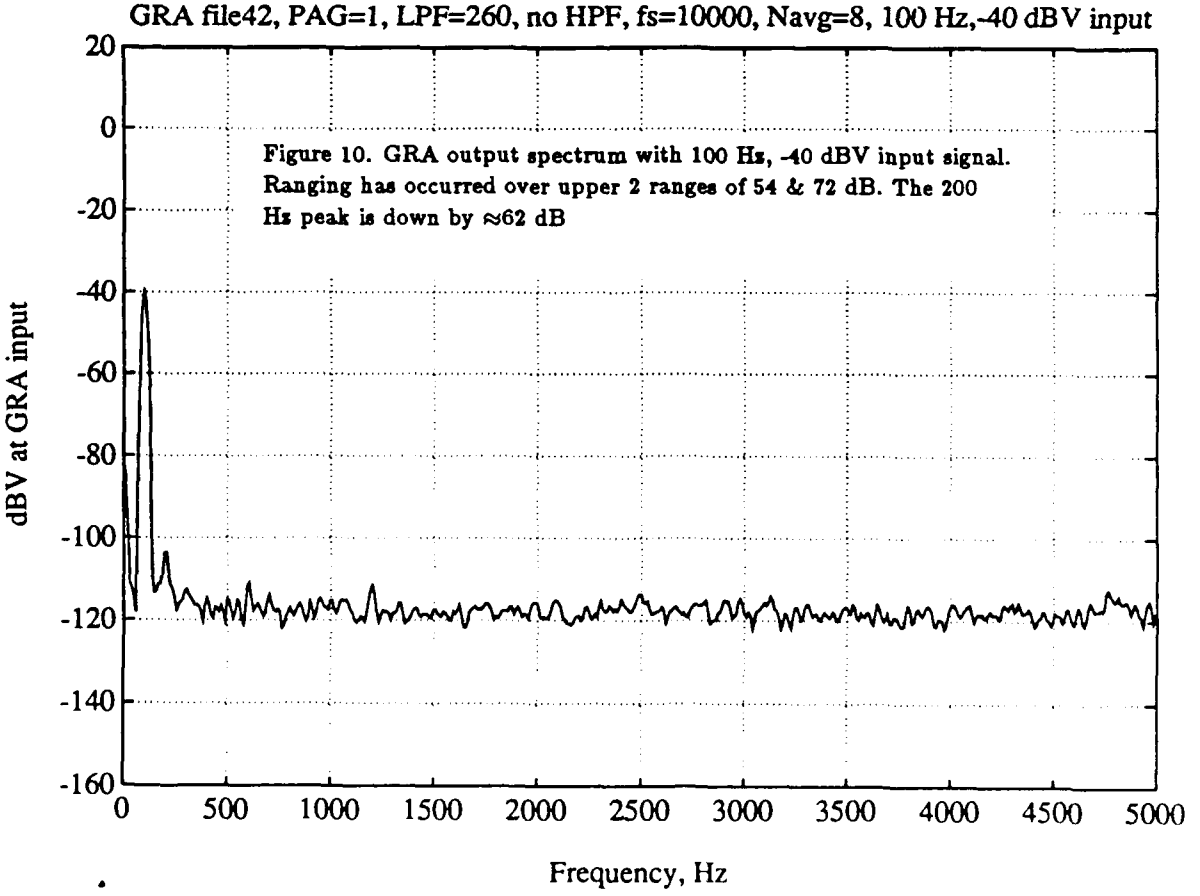


Figure 10. GRA output spectrum with 100 Hz, -40 dBV input signal. Ranging has occurred over upper 2 ranges of 54 & 72 dB. The 200 Hz peak is down by ≈62 dB

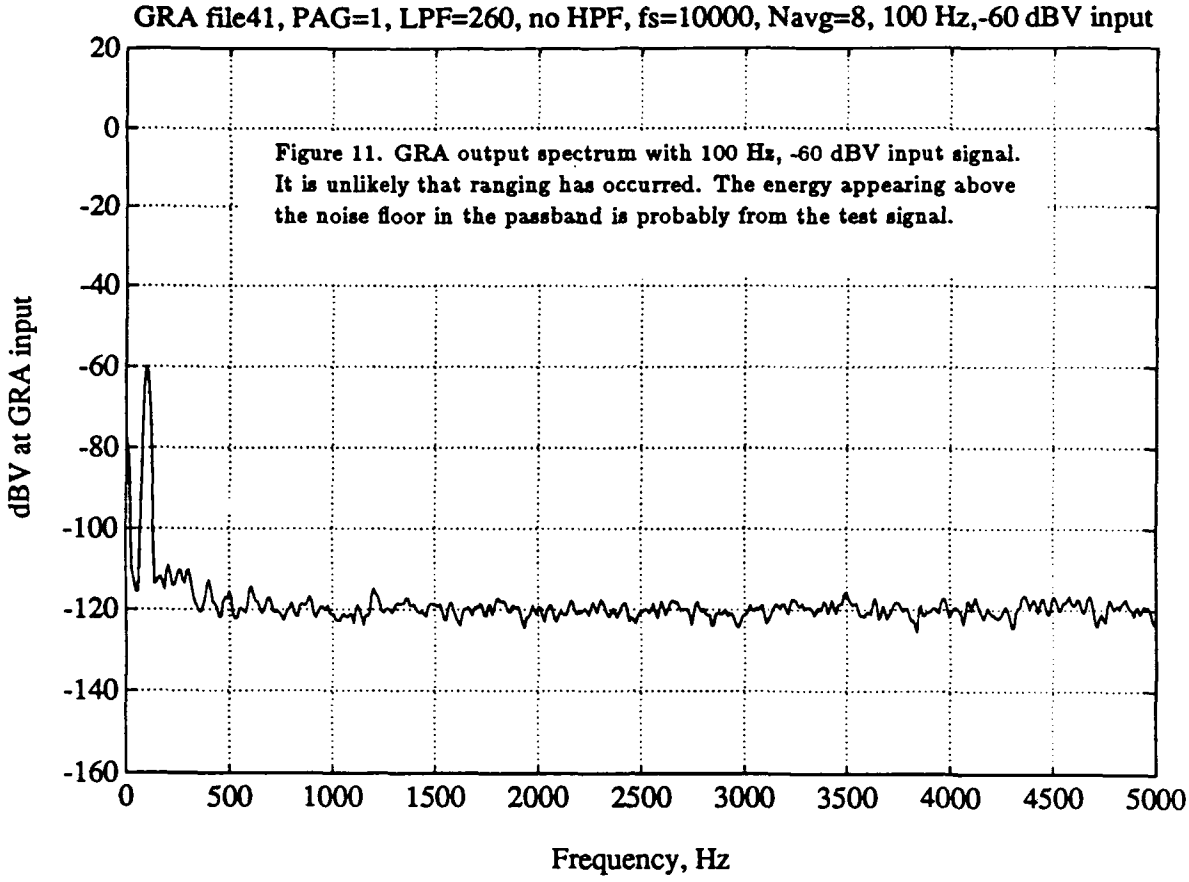


Figure 11. GRA output spectrum with 100 Hz, -60 dBV input signal. It is unlikely that ranging has occurred. The energy appearing above the noise floor in the passband is probably from the test signal.

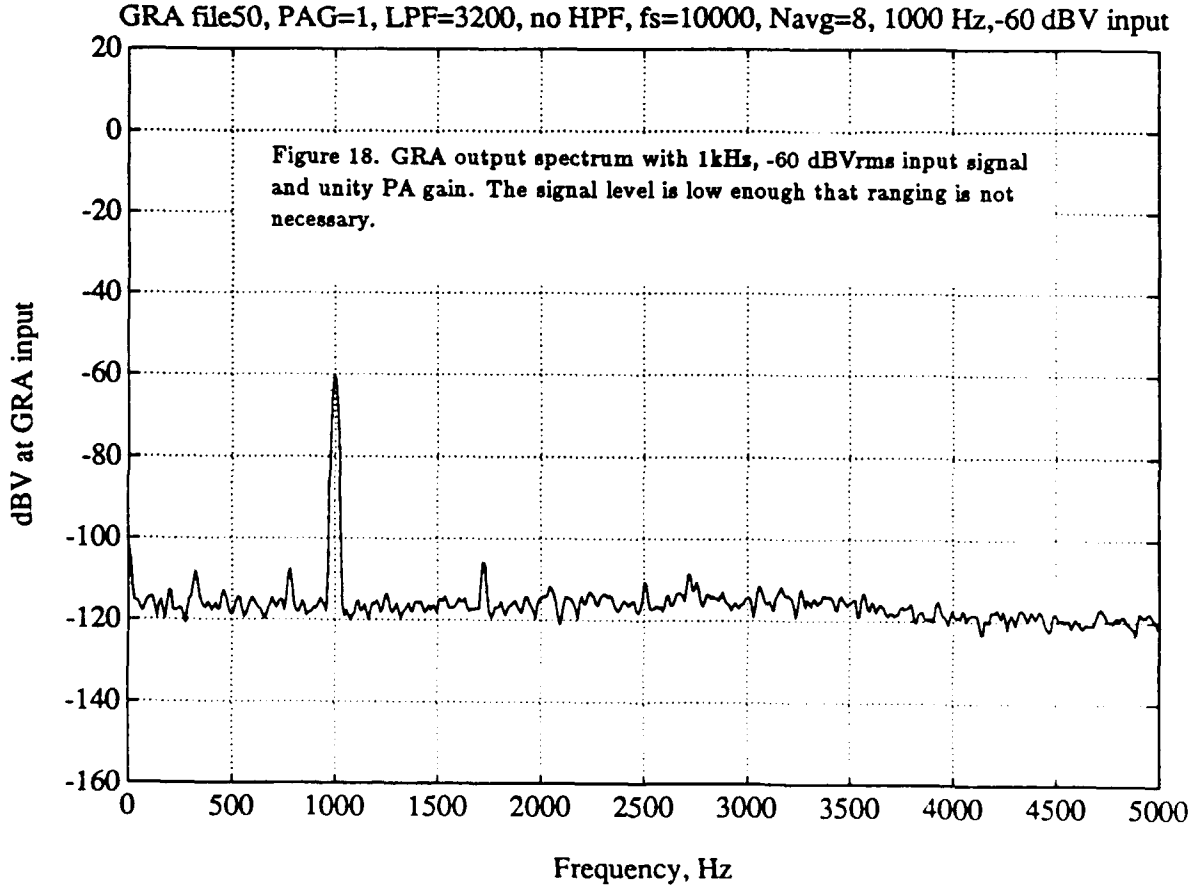


Figure 18. GRA output spectrum with 1kHz, -60 dBVrms input signal and unity PA gain. The signal level is low enough that ranging is not necessary.

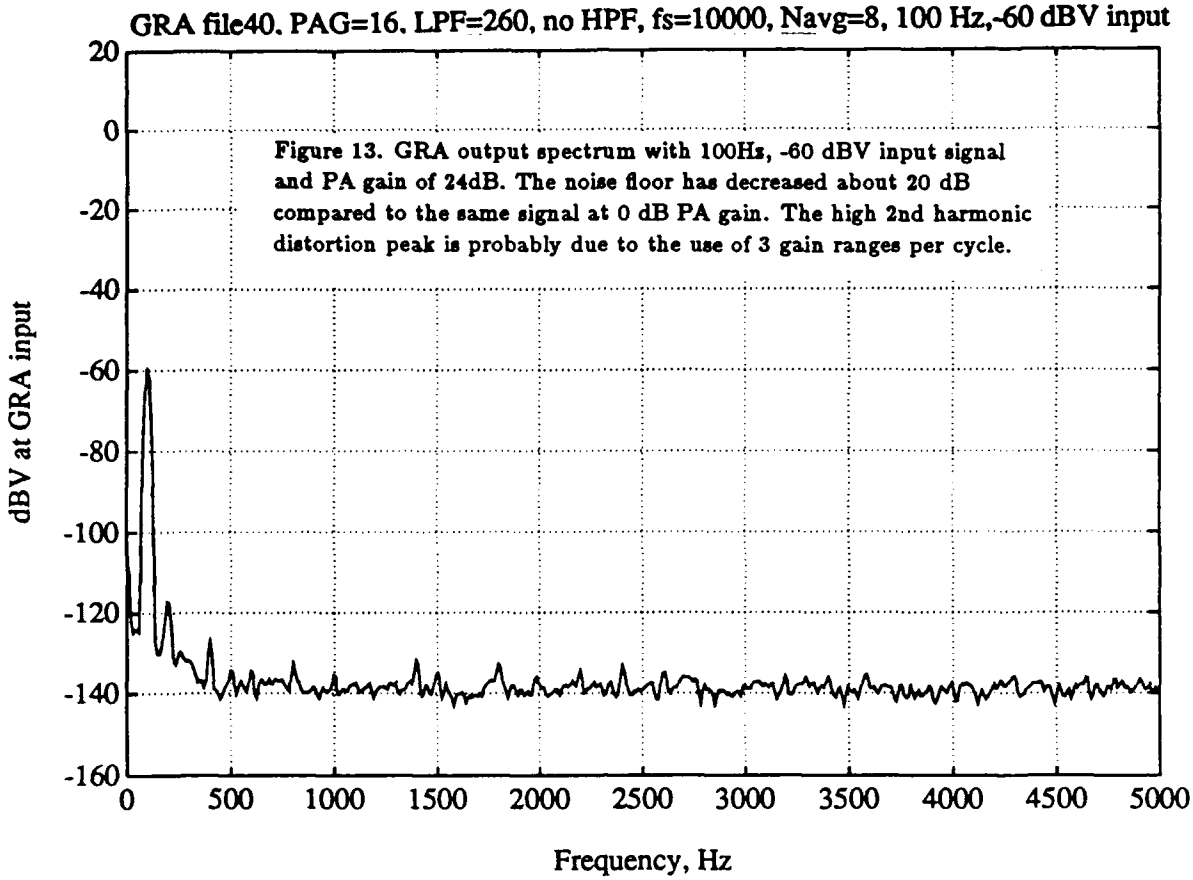


Figure 13. GRA output spectrum with 100Hz, -60 dBV input signal and PA gain of 24dB. The noise floor has decreased about 20 dB compared to the same signal at 0 dB PA gain. The high 2nd harmonic distortion peak is probably due to the use of 3 gain ranges per cycle.

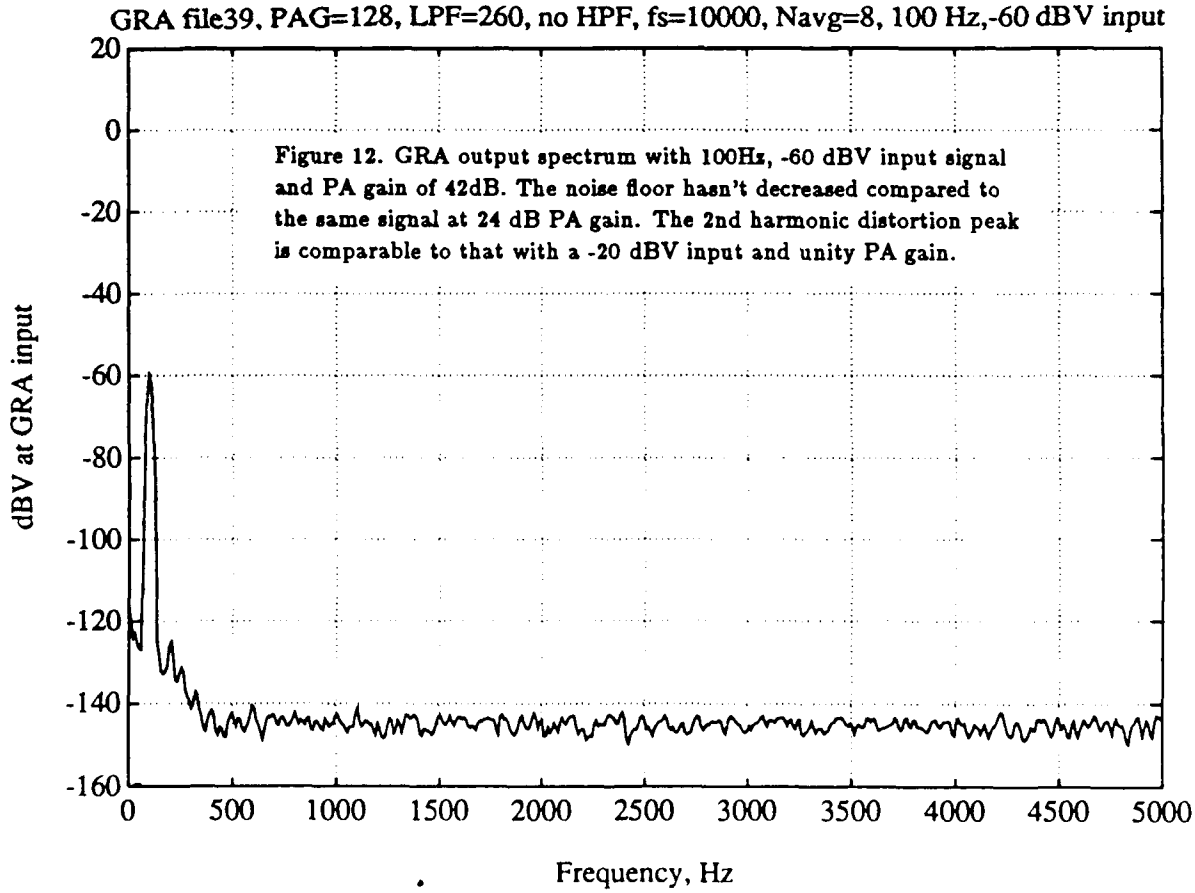


Figure 12. GRA output spectrum with 100Hz, -60 dBV input signal and PA gain of 42dB. The noise floor hasn't decreased compared to the same signal at 24 dB PA gain. The 2nd harmonic distortion peak is comparable to that with a -20 dBV input and unity PA gain.

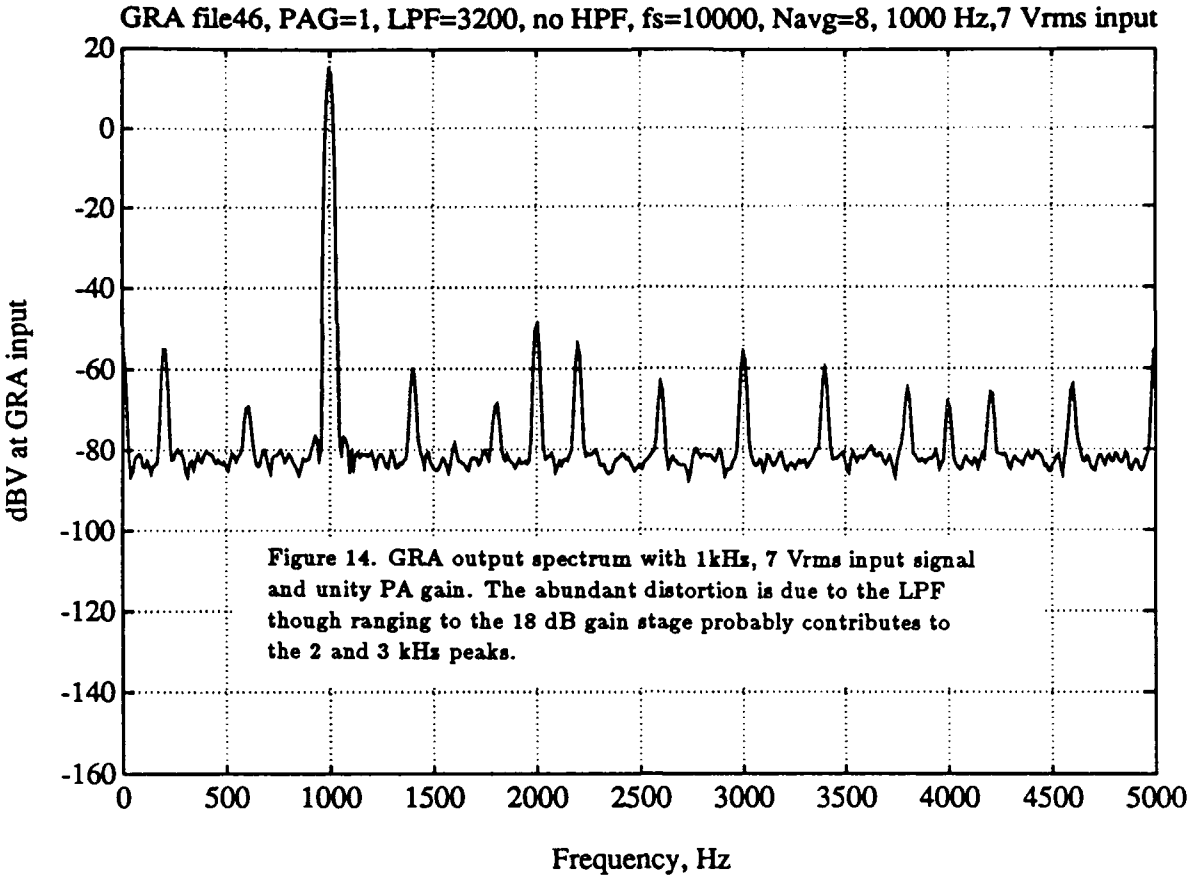


Figure 14. GRA output spectrum with 1kHz, 7 Vrms input signal and unity PA gain. The abundant distortion is due to the LPF though ranging to the 18 dB gain stage probably contributes to the 2 and 3 kHz peaks.

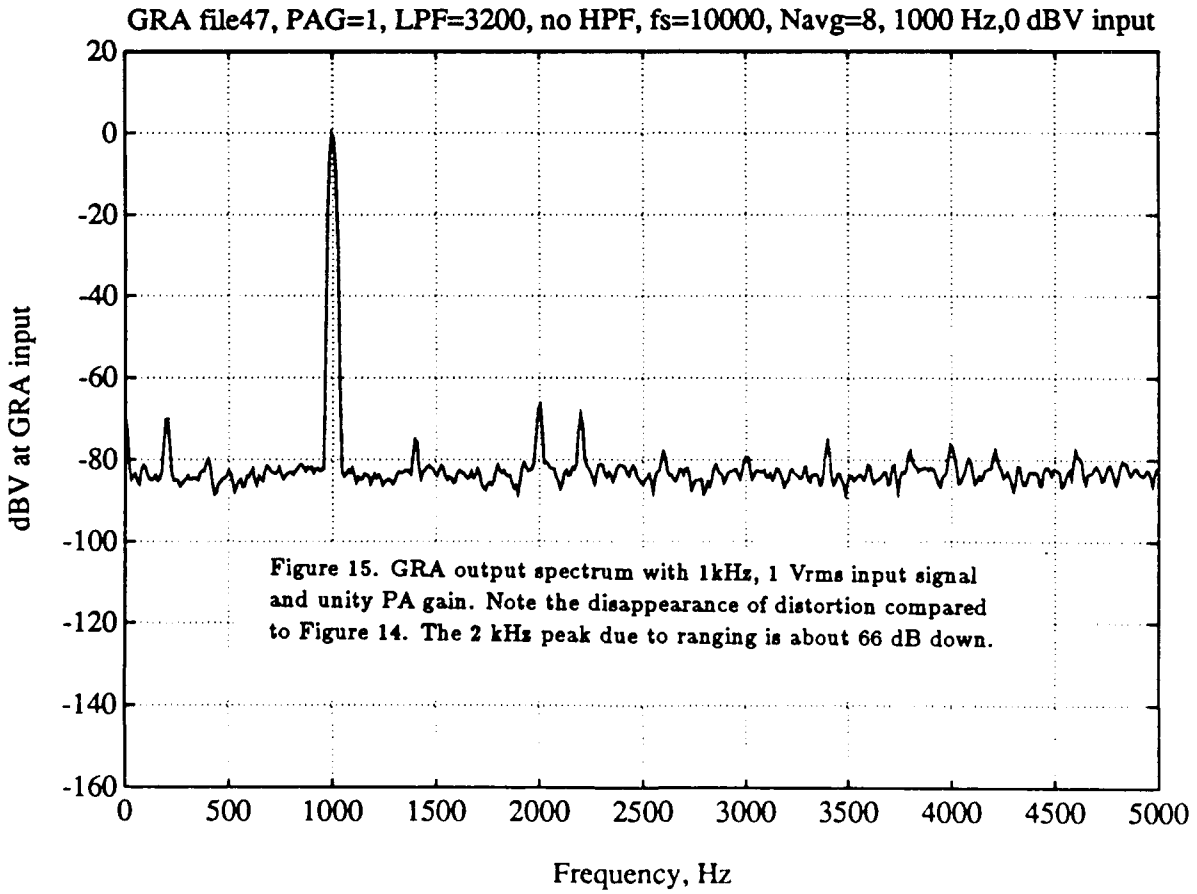


Figure 15. GRA output spectrum with 1kHz, 1 Vrms input signal and unity PA gain. Note the disappearance of distortion compared to Figure 14. The 2 kHz peak due to ranging is about 66 dB down.

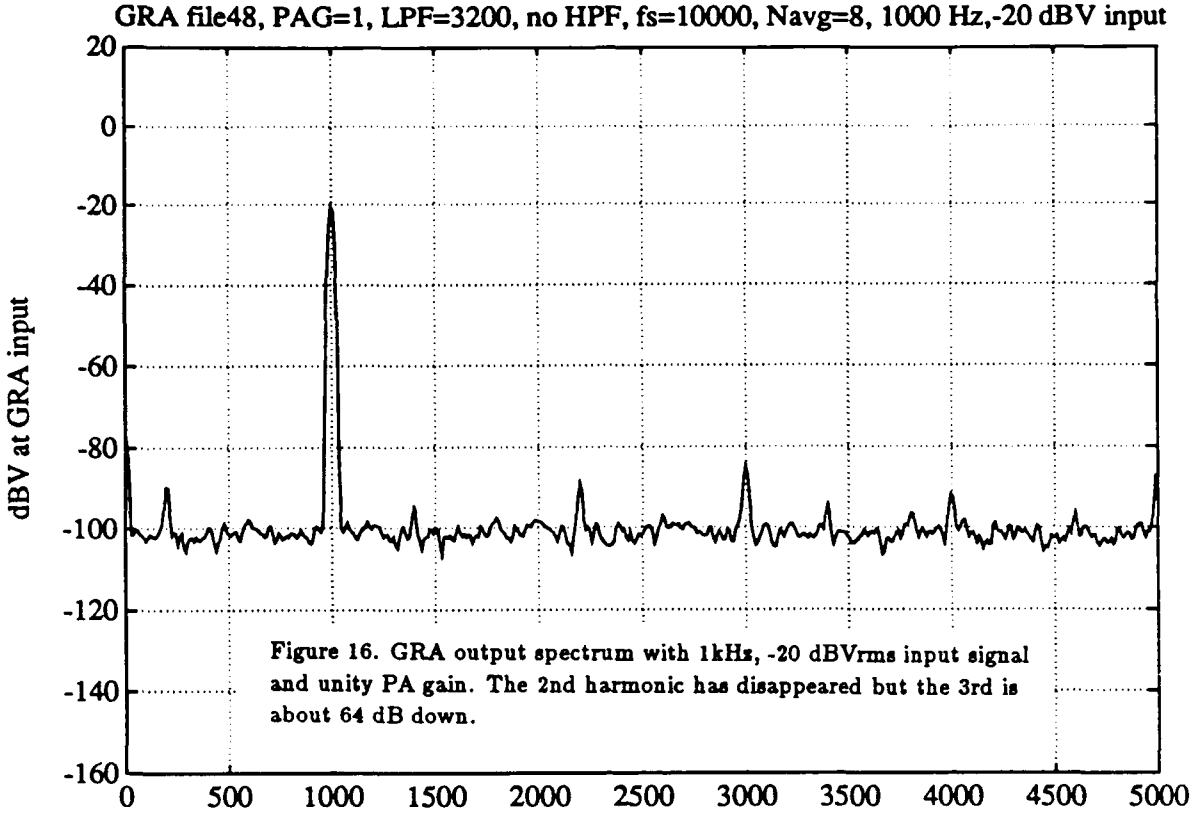


Figure 16. GRA output spectrum with 1kHz, -20 dBVrms input signal and unity PA gain. The 2nd harmonic has disappeared but the 3rd is about 64 dB down.

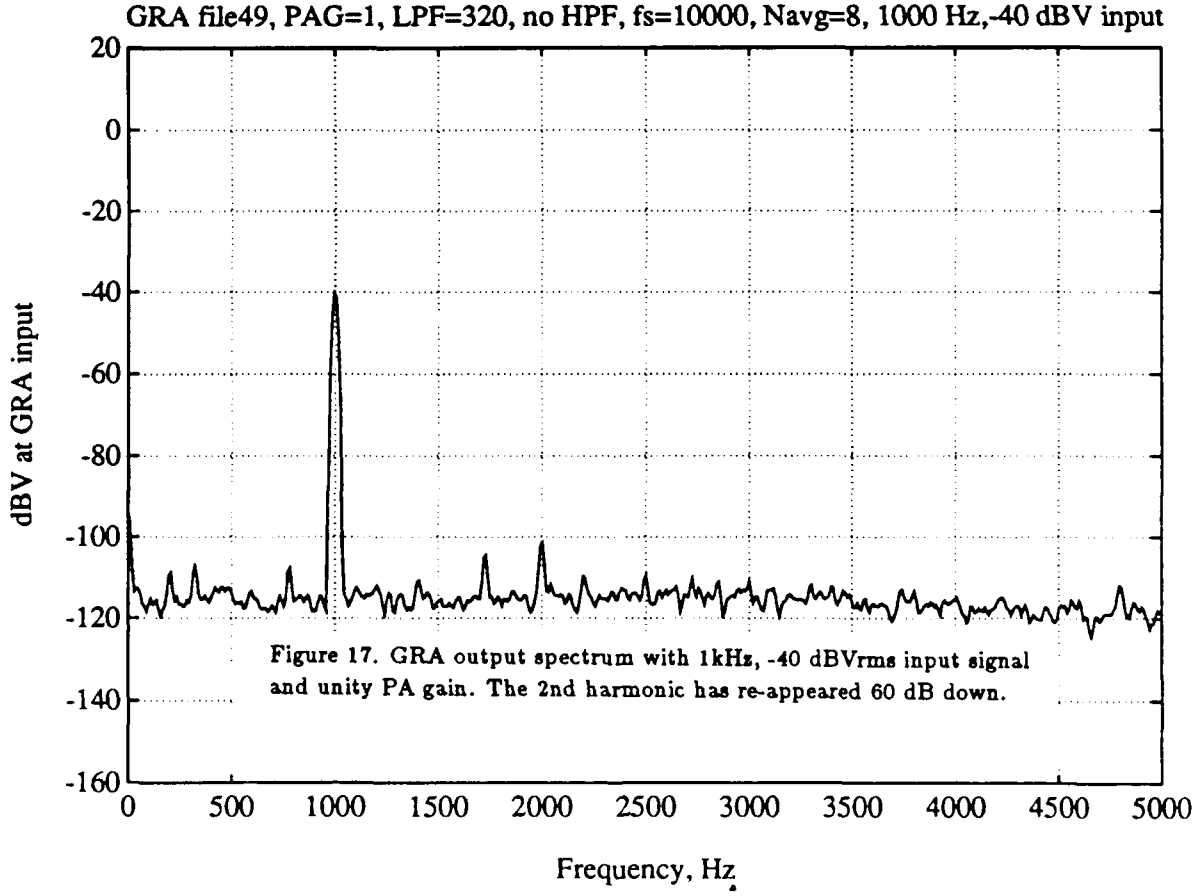


Figure 17. GRA output spectrum with 1kHz, -40 dBVrms input signal and unity PA gain. The 2nd harmonic has re-appeared 60 dB down.

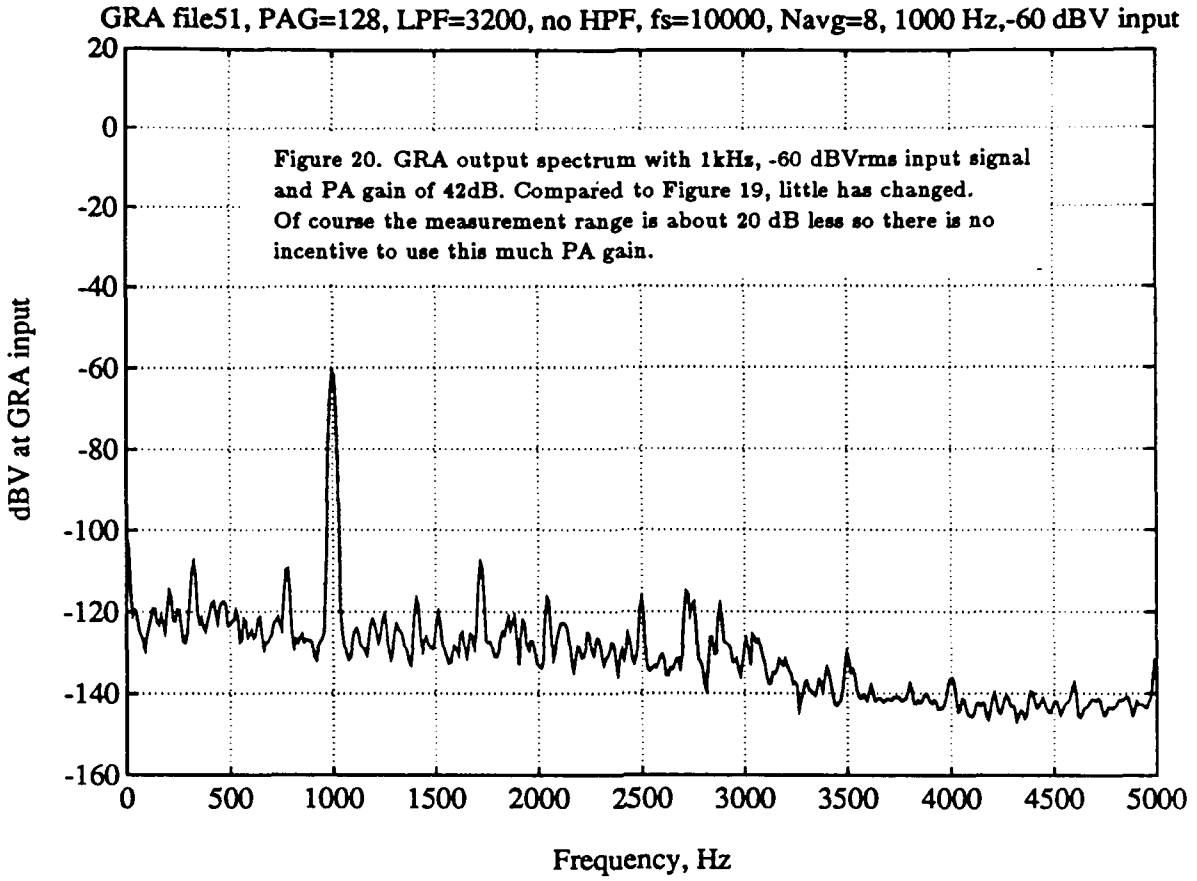


Figure 20. GRA output spectrum with 1kHz, -60 dBVrms input signal and PA gain of 42dB. Compared to Figure 19, little has changed. Of course the measurement range is about 20 dB less so there is no incentive to use this much PA gain.

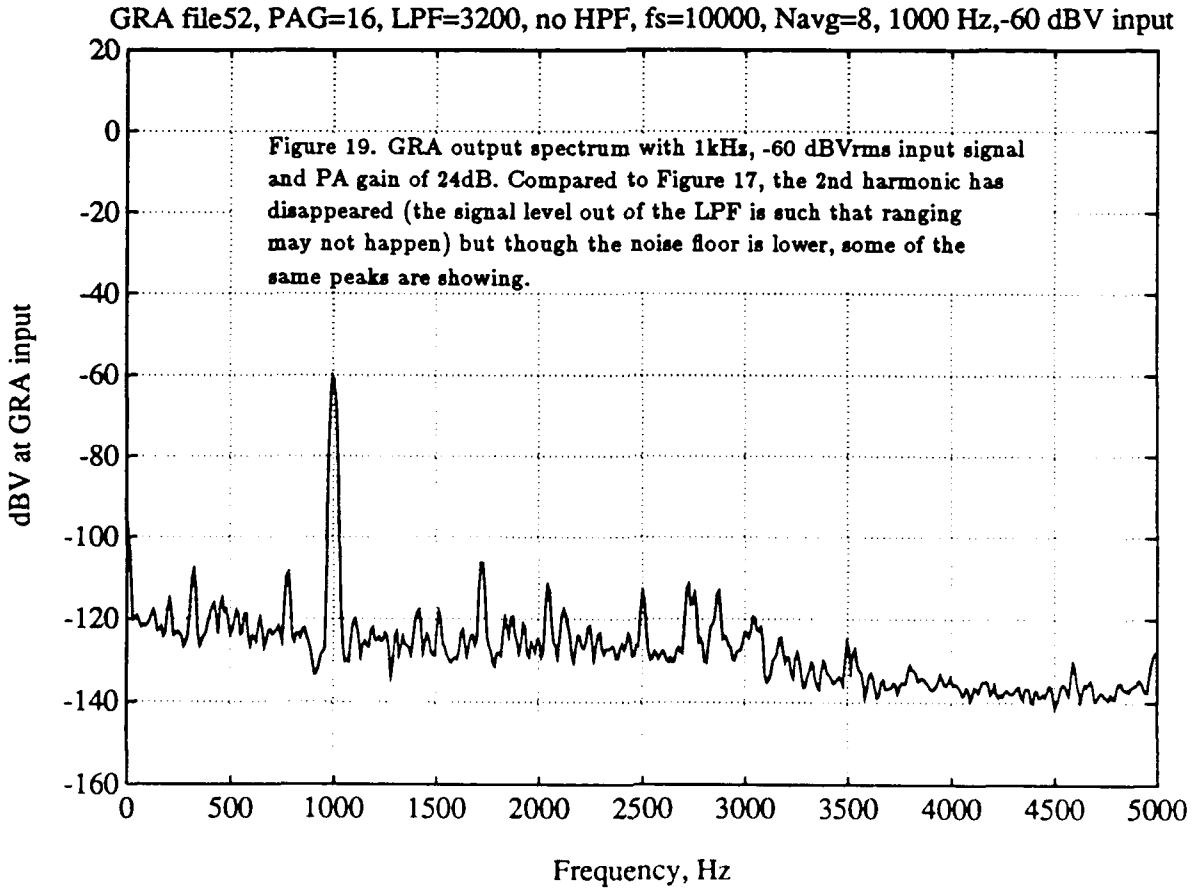


Figure 19. GRA output spectrum with 1kHz, -60 dBVrms input signal and PA gain of 24dB. Compared to Figure 17, the 2nd harmonic has disappeared (the signal level out of the LPF is such that ranging may not happen) but though the noise floor is lower, some of the same peaks are showing.

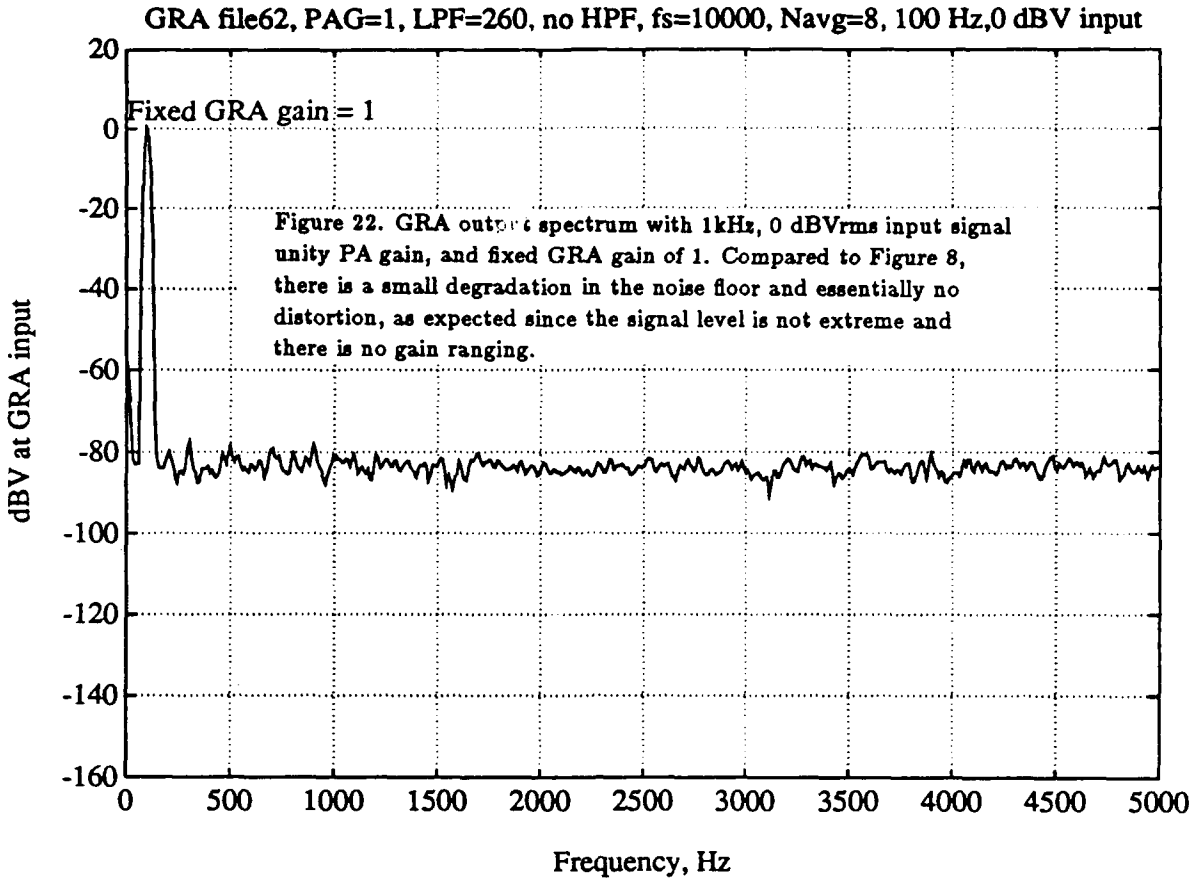


Figure 22. GRA output spectrum with 1kHz, 0 dBVrms input signal unity PA gain, and fixed GRA gain of 1. Compared to Figure 8, there is a small degradation in the noise floor and essentially no distortion, as expected since the signal level is not extreme and there is no gain ranging.

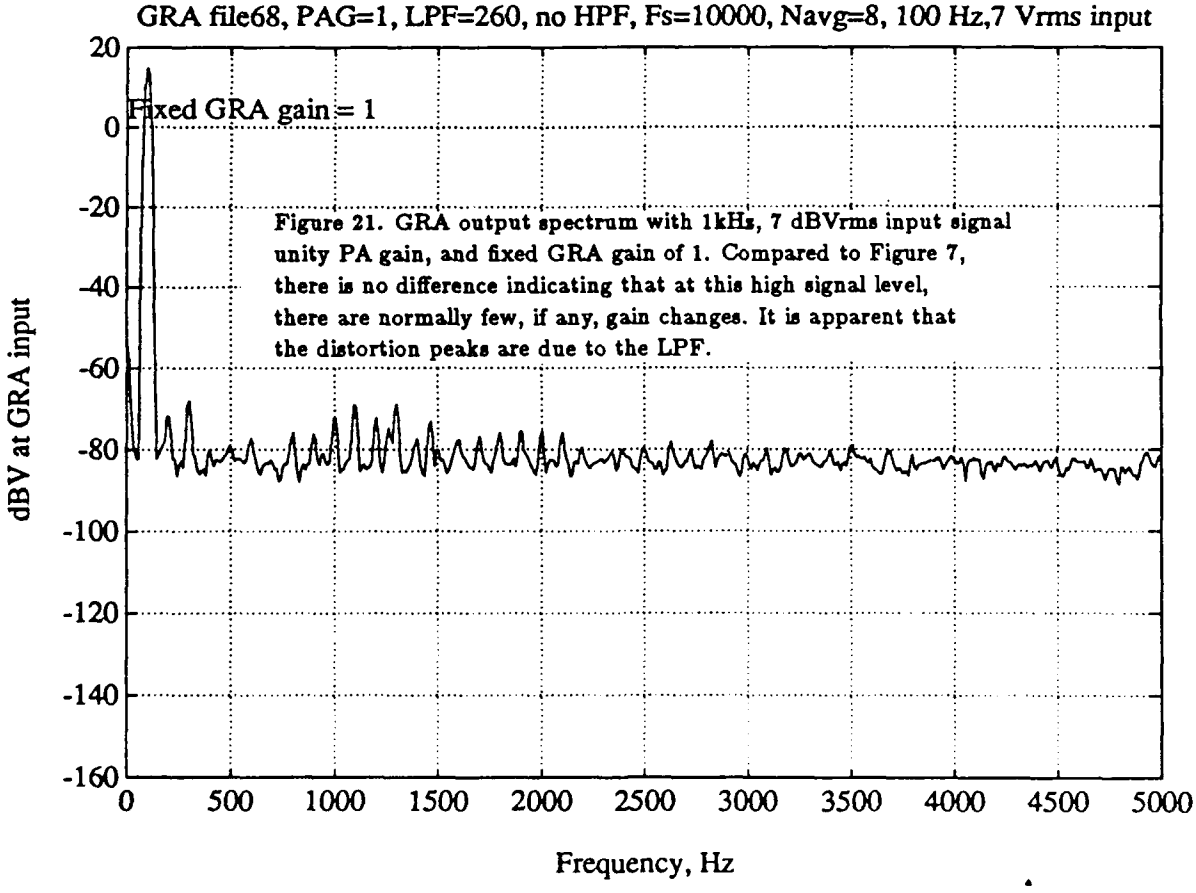


Figure 21. GRA output spectrum with 1kHz, 7 dBVrms input signal unity PA gain, and fixed GRA gain of 1. Compared to Figure 7, there is no difference indicating that at this high signal level, there are normally few, if any, gain changes. It is apparent that the distortion peaks are due to the LPF.

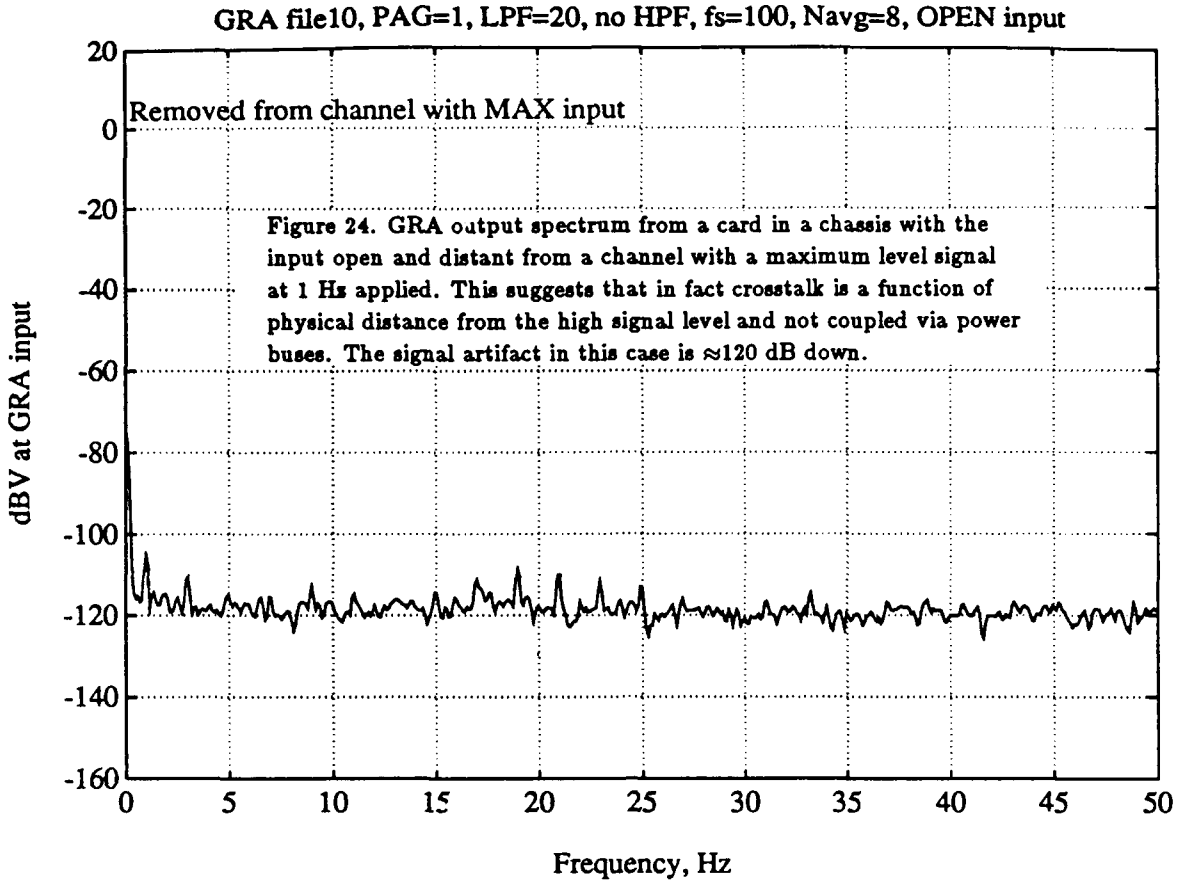


Figure 24. GRA output spectrum from a card in a chassis with the input open and distant from a channel with a maximum level signal at 1 Hz applied. This suggests that in fact crosstalk is a function of physical distance from the high signal level and not coupled via power buses. The signal artifact in this case is ≈120 dB down.

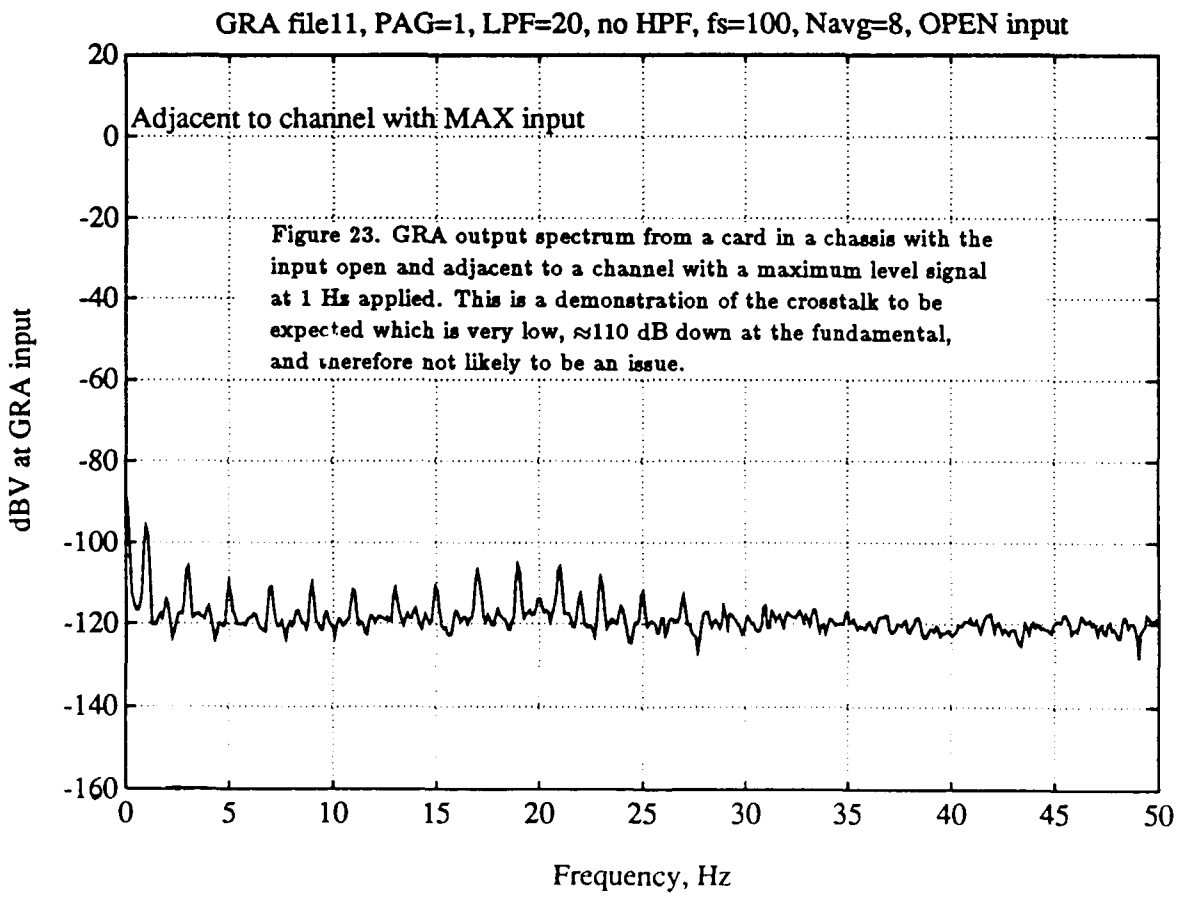


Figure 23. GRA output spectrum from a card in a chassis with the input open and adjacent to a channel with a maximum level signal at 1 Hz applied. This is a demonstration of the crosstalk to be expected which is very low, ≈110 dB down at the fundamental, and therefore not likely to be an issue.

WHOI MULTI-CHANNEL DATA ACQUISITION SYSTEM

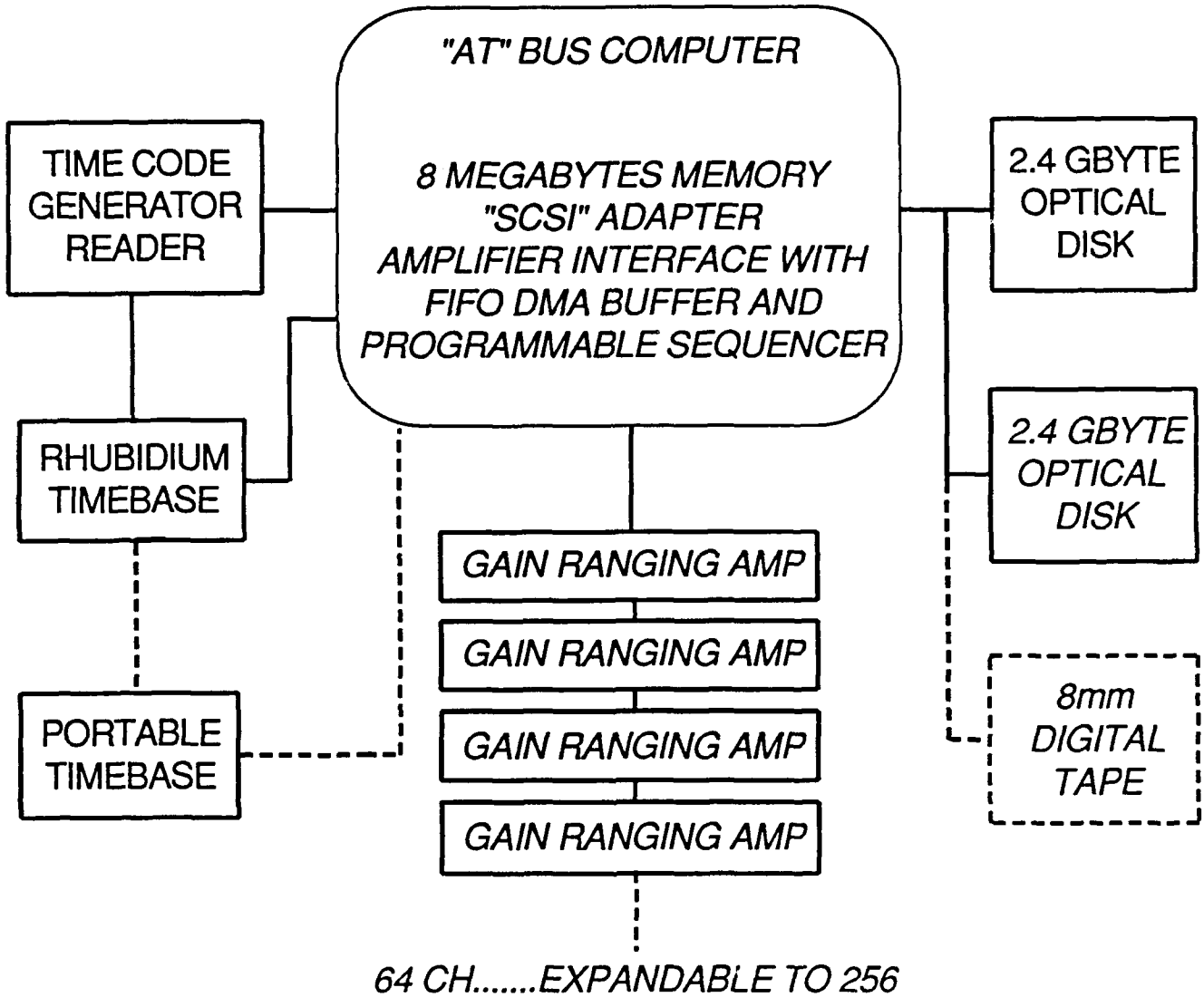


Figure 25. Multi-channel Acquisition System Block Diagram

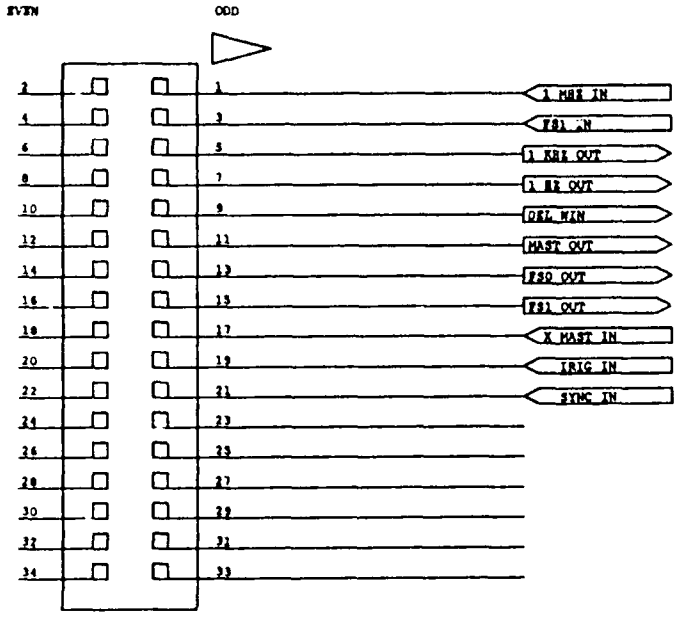


Figure 27. GRA Interface Acquisition Parameter I/O

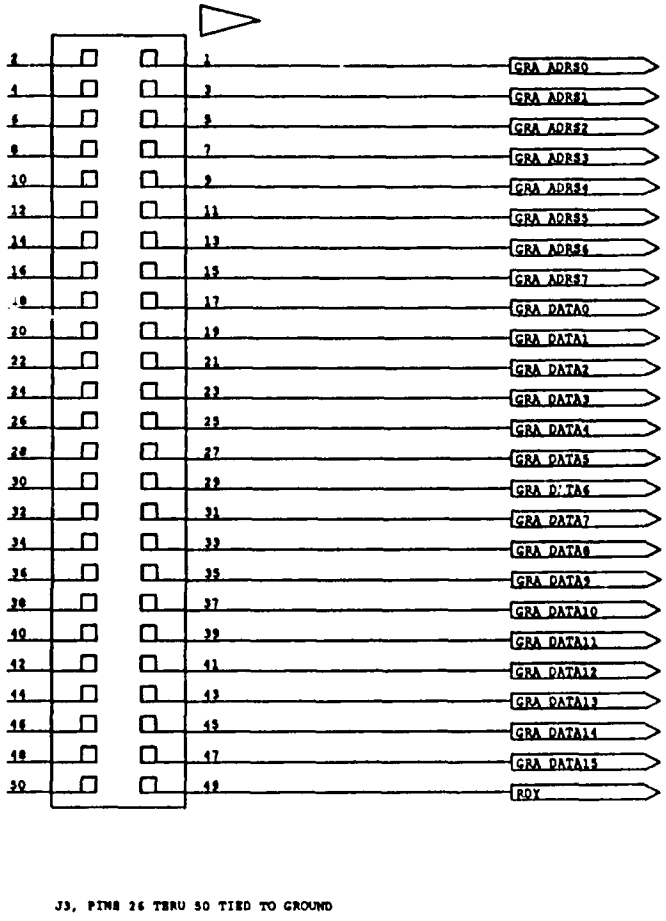


Figure 26. GRA Interface Data/Control Bus Connector

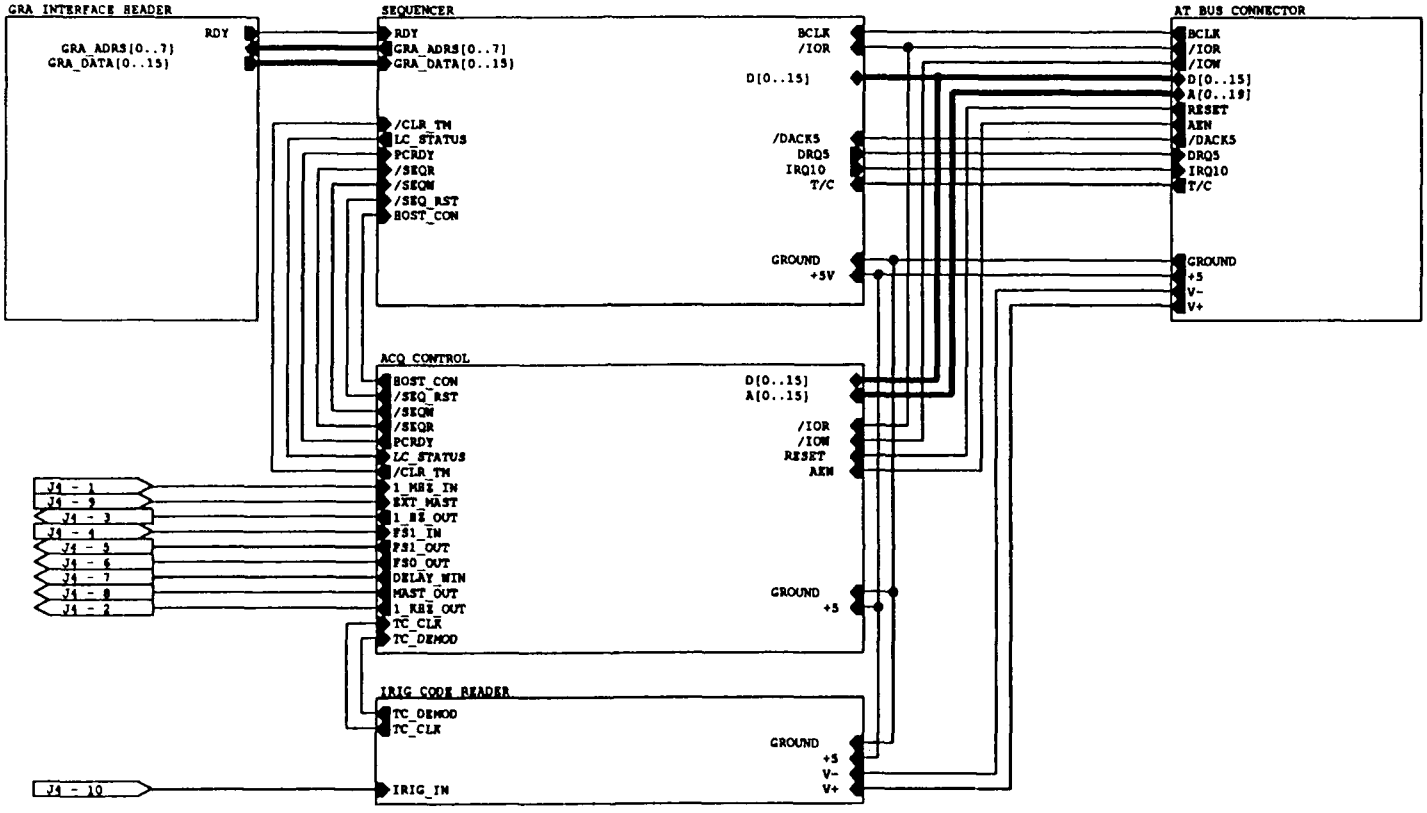


Figure 28. GRA Interface Block Diagram

VON DER HEYDT		
Size A	Document Number AT BUS GRA CONTROLLER, BLOCK DIAGRAM	REV A
Date: December 4, 1989	Sheet 1 of 7	

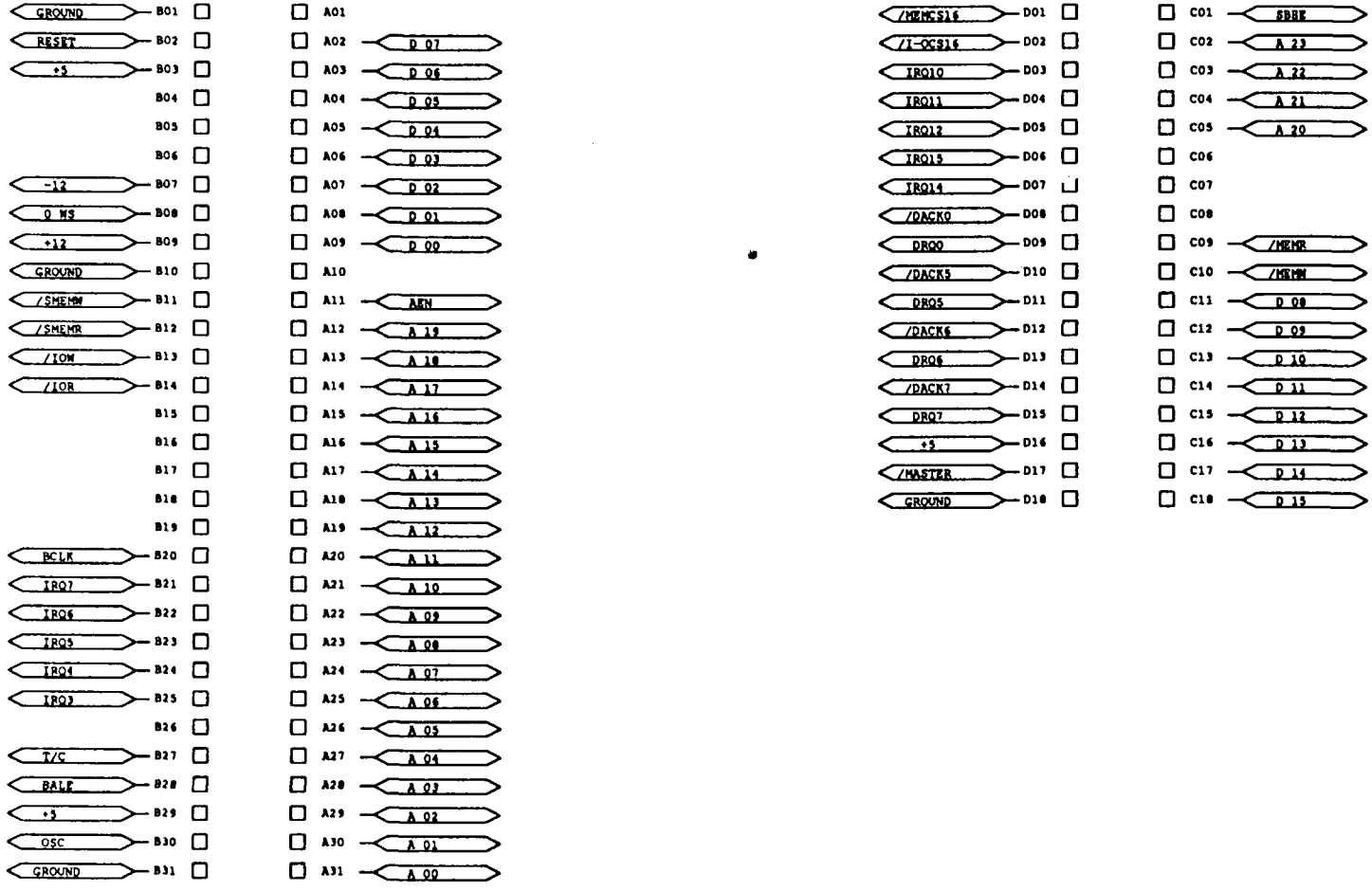


Figure 29. PC/AT (ISA) Bus Signals

AT BUS GRA CONTROLLER - von der Heydt		
Size A	Document Number AT BUS USAGE BY CONTROLLER	REV A
Date: November 7, 1989	Sheet 2 of 7	

GRA CARD 100 PIN CON (CARD & BACKPLANE)			50 PIN BLUE RIBBON CON (GRA BACKPANEL ONLY)		50 PIN HEADER CON (ATBUS INTERFACE ONLY)		INTERFACE TO OLD GRA (VIA SCRAMBLER BOX)	
100 PIN		FUNCTION	50 PIN BLUE RIBBON		50 PIN HEADER		50 PIN B.R.	
1	2	+5D						
3	4	+5D						
5	6	DIG GND						
7	8	DIG GND						
9	10	DIG GND						
11	12	ADRS 0	1		1		41	RD CLK
13	14	ADRS 1	2		3			
15	16	ADRS 2	3		5			
17	18	ADRS 3	4		7			
19	20	ADRS 4	5		9			
21	22	ADRS 5	6		11			
23	24	ADRS 6	7		13		39	CS0
25	26	ADRS 7	8		15		40	CS1
27	28	D0	9		17		27	
29	30	D1	10		19		28	
31	32	D2	11		21		29	
33	34	D3	12		23		30	
35	36	D4	13		25		31	
37	38	D5	14		27		32	
39	40	D6	15		29		33	
41	42	D7	16		31		34	
43	44	D8	17		33		43	
45	46	D9	18		35		44	
47	48	D10	19		37		45	
49	50	D11	20		39		46	
51	52	D12	21		41		47	
53	54	D13	22		43		48	
55	56	D14	23		45		49	
57	58	D15	24		47		50	
59	60	RDY	25		49		26	
61	62	FS	PINS 26 - 50		EVEN # PINS		PINS 1 - 25	
63	64	SCOM	GROUND		GROUND		GROUND	
65	66							
67	68							
69	70	AGND						
71	72	ALCAL						
73	74	AGND						
75	76	AGND						
77	78	-5A						
79	80	-5A						
81	82	+5A						
83	84	+5A						
85	86	V-						
87	88	V-						
89	90	V+						
91	92	V+						
93	94	SIG GND						
95	96	SIG GND						
97	98	SIGNAL						
99	100	SIGNAL						

Figure 30. Signal Connections Between GRA Chassis and PC Interface

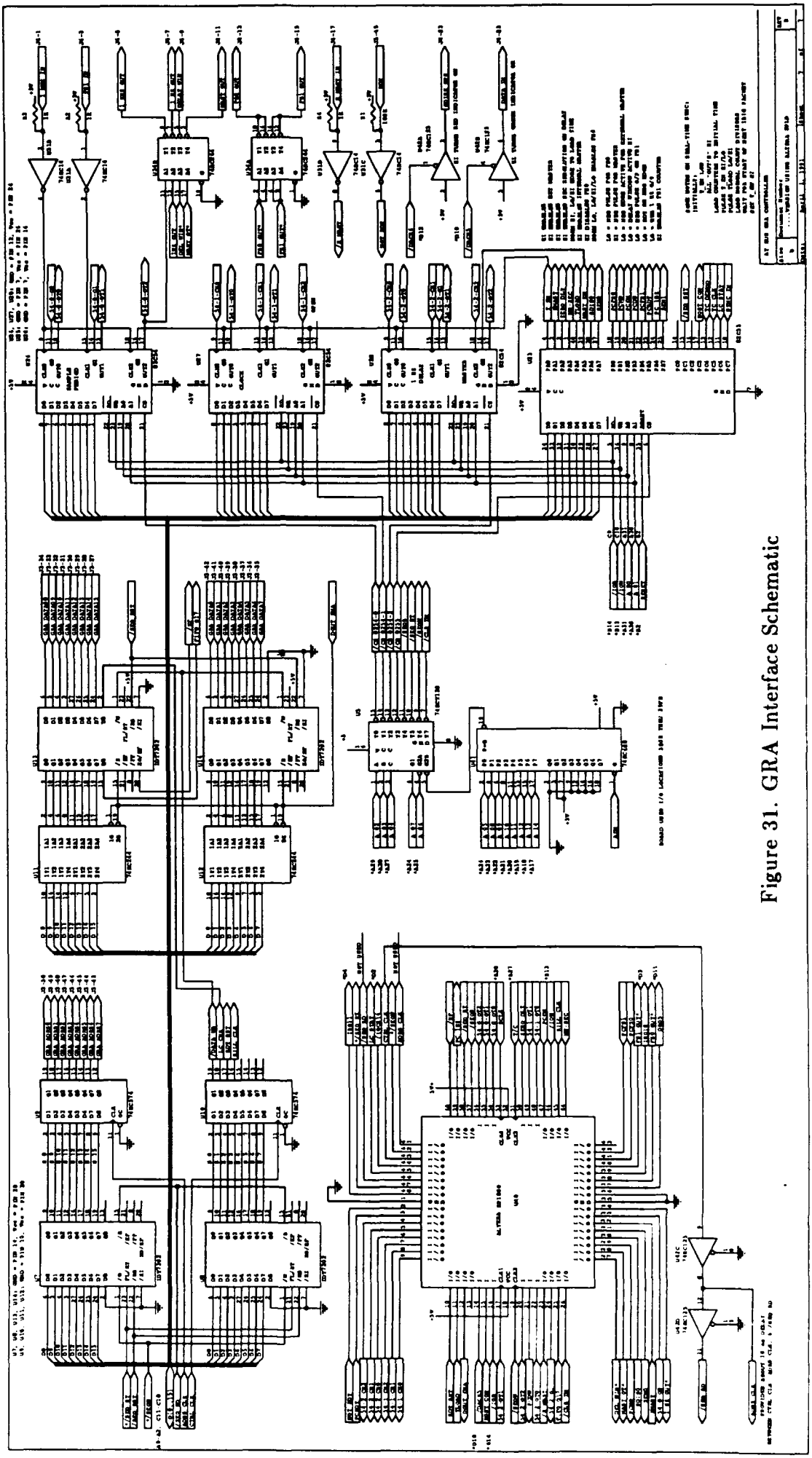


Figure 31. GRA Interface Schematic

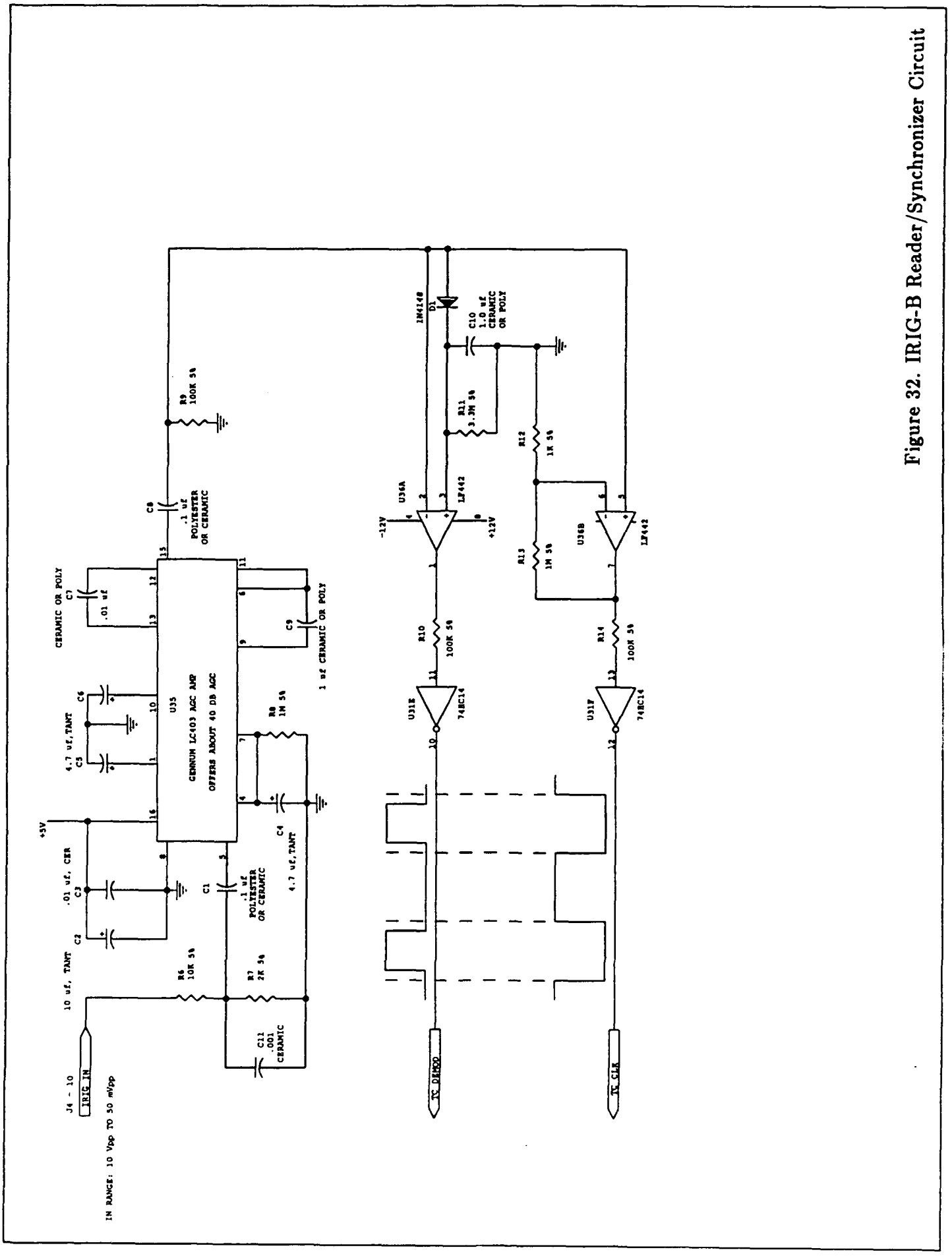


Figure 32. IRIG-B Reader/Synchronizer Circuit

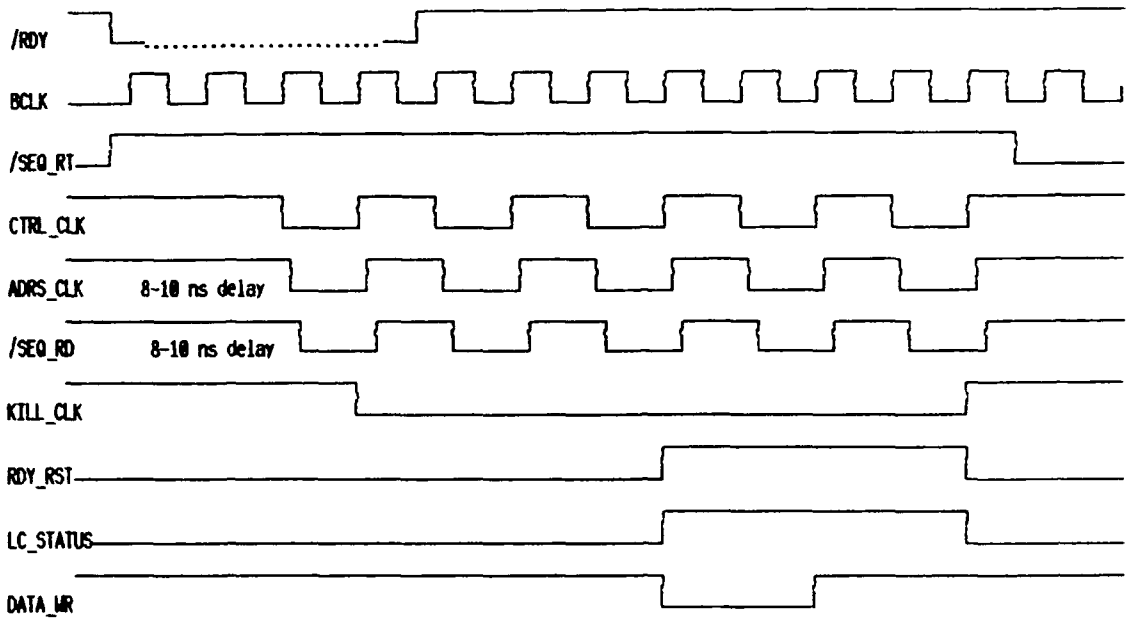


Figure 33. Shown are the important GRA interface sequencer logic signals and their relative timing during input of data from a single GRA channel. The */RDY* signal from the GRA's initiates the process when its falling edge occurs. *BCLK* has a 125 ns period on a standard ISA bus, which is divided by 2 to give the *CTRL_CLK, ADRS_CLK, and /SEQ_RD* signals a 250 ns sequencer period. With a single channel (or the last channel when more than one are used) an extra half sequencer cycle is required to start and finish the process. *KILL_CLK, RDY_RST, LC_STATUS, and DATA_WR* are sequencer outputs that control the transfer of samples from the GRA data bus to the GRA interface FIFO buffer. A 2 byte sample is transferred in 1 μs with an 8 MHz *BCLK*.

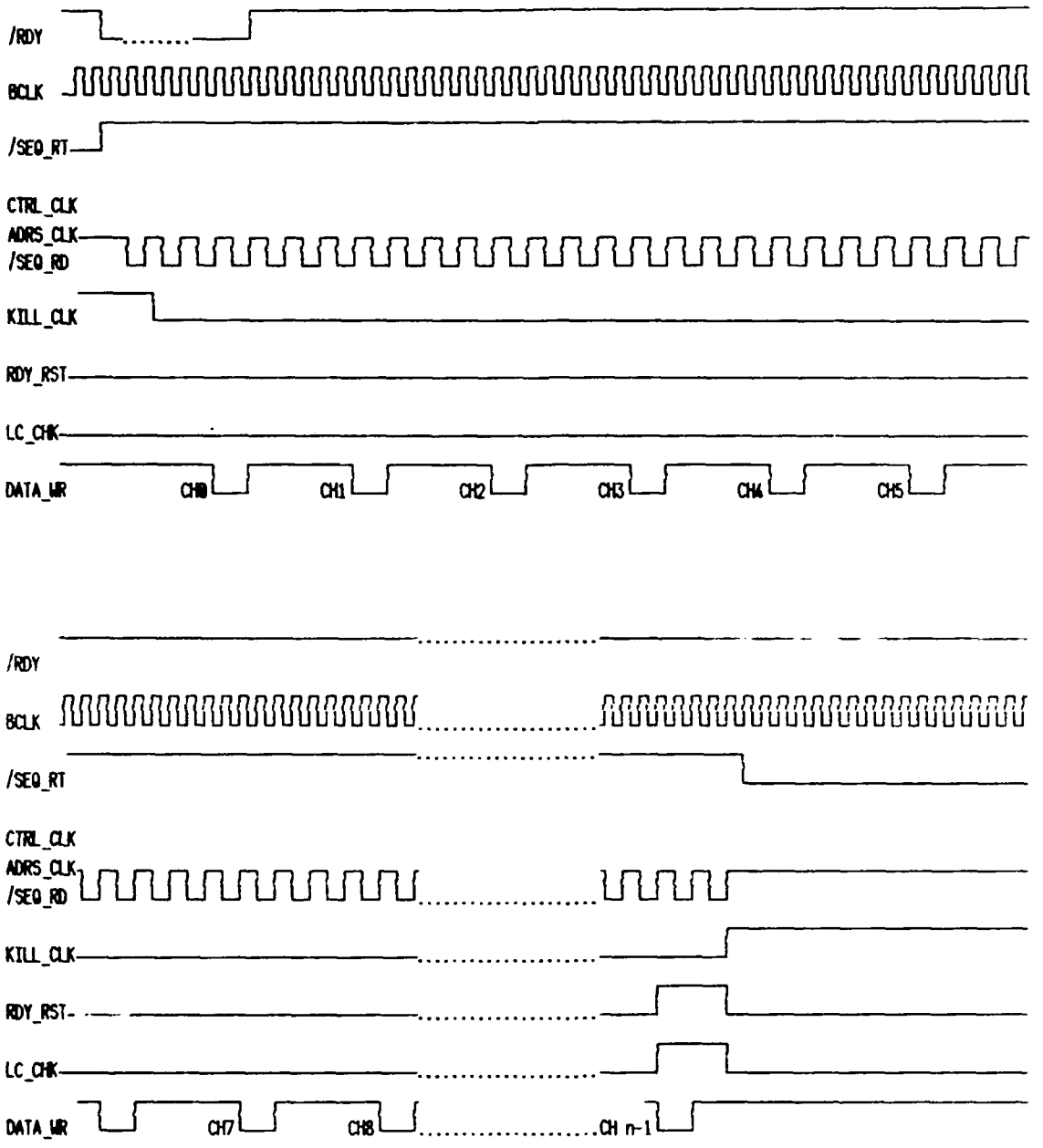


Figure 34. Sequencer Timing Diagram, "n" Channels

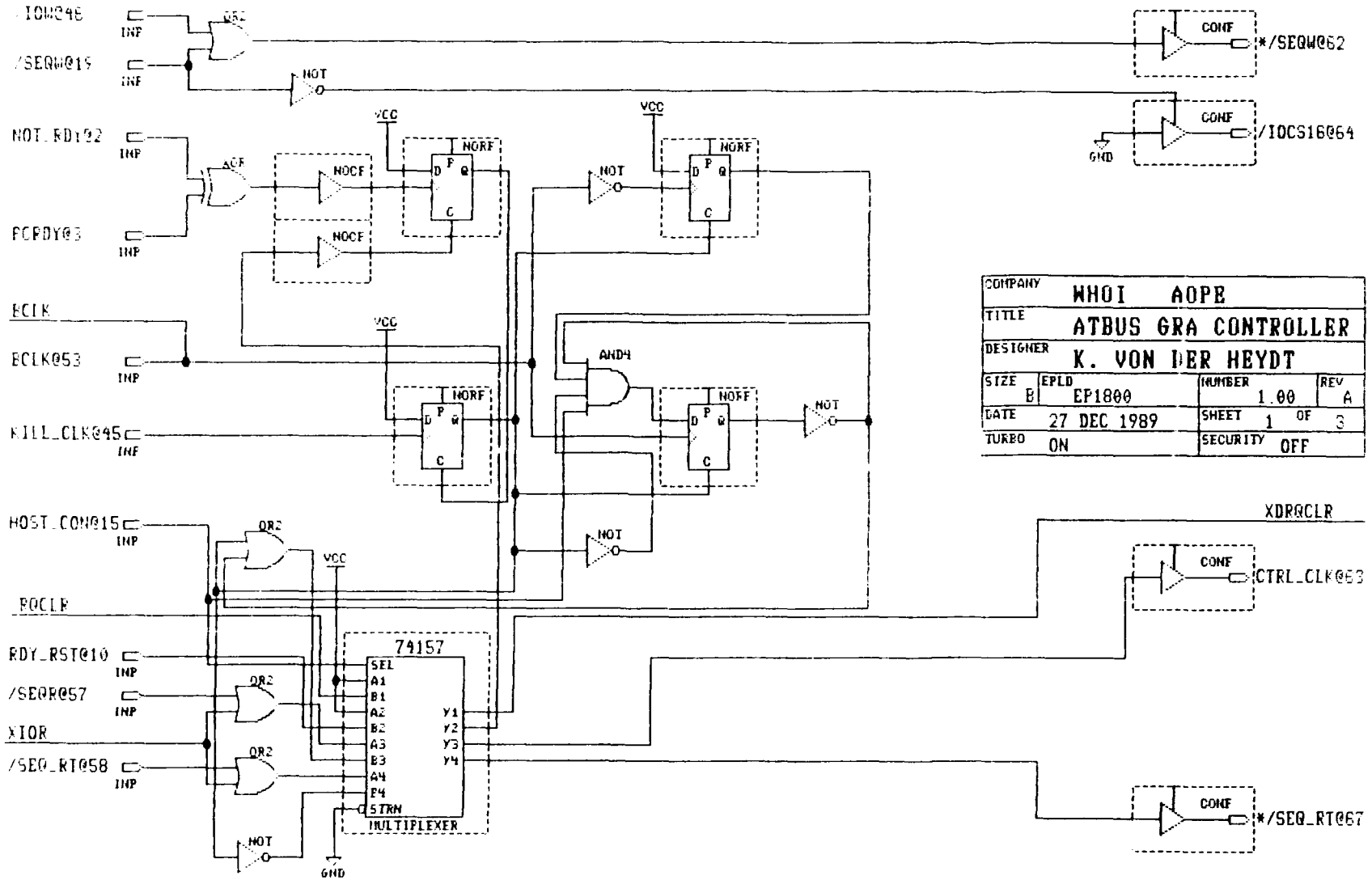


Figure 35. Altera PLD, Sequencer timing & Control

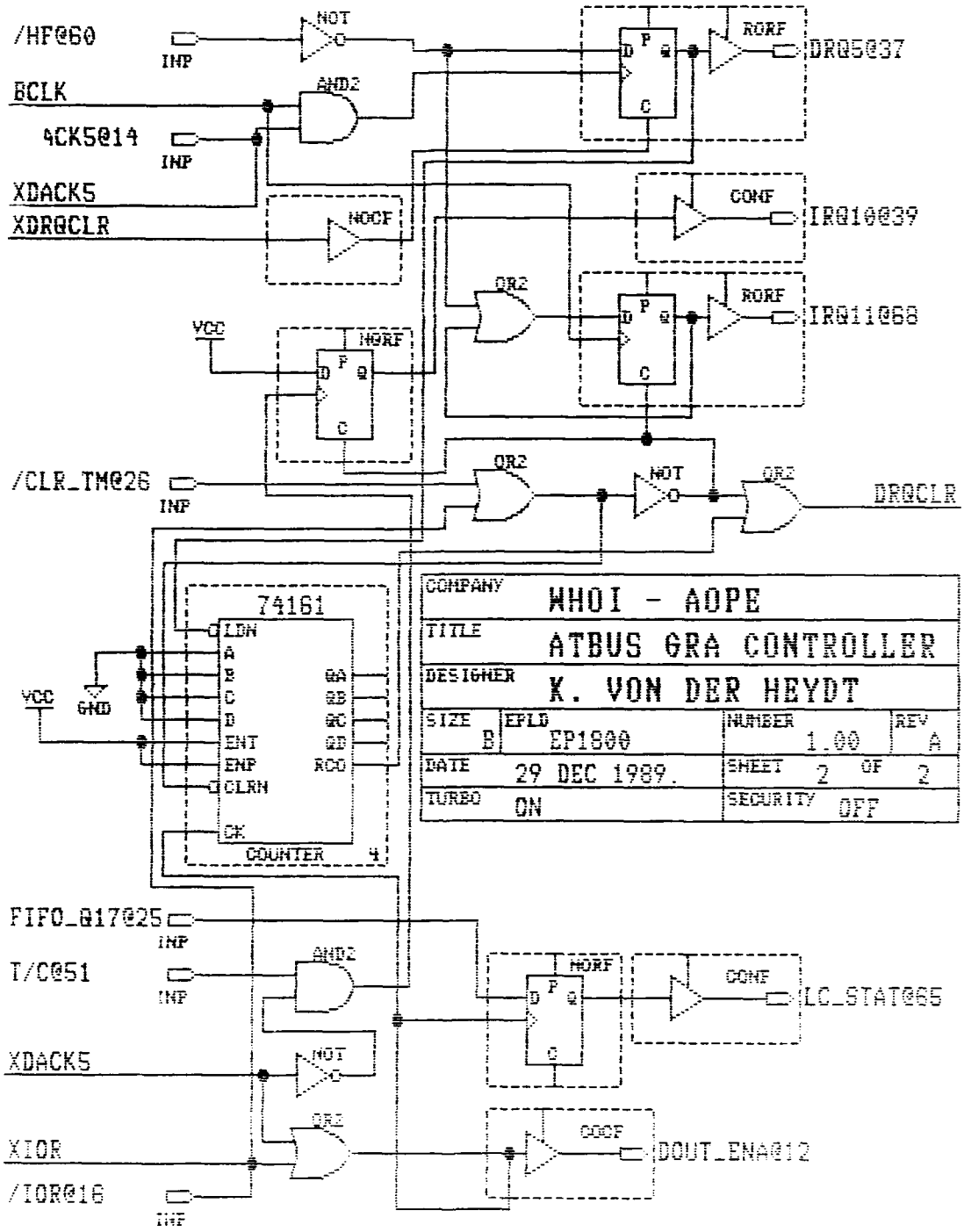


Figure 36. Altera PLD, Sequencer DMA Reload & Interrupt Control

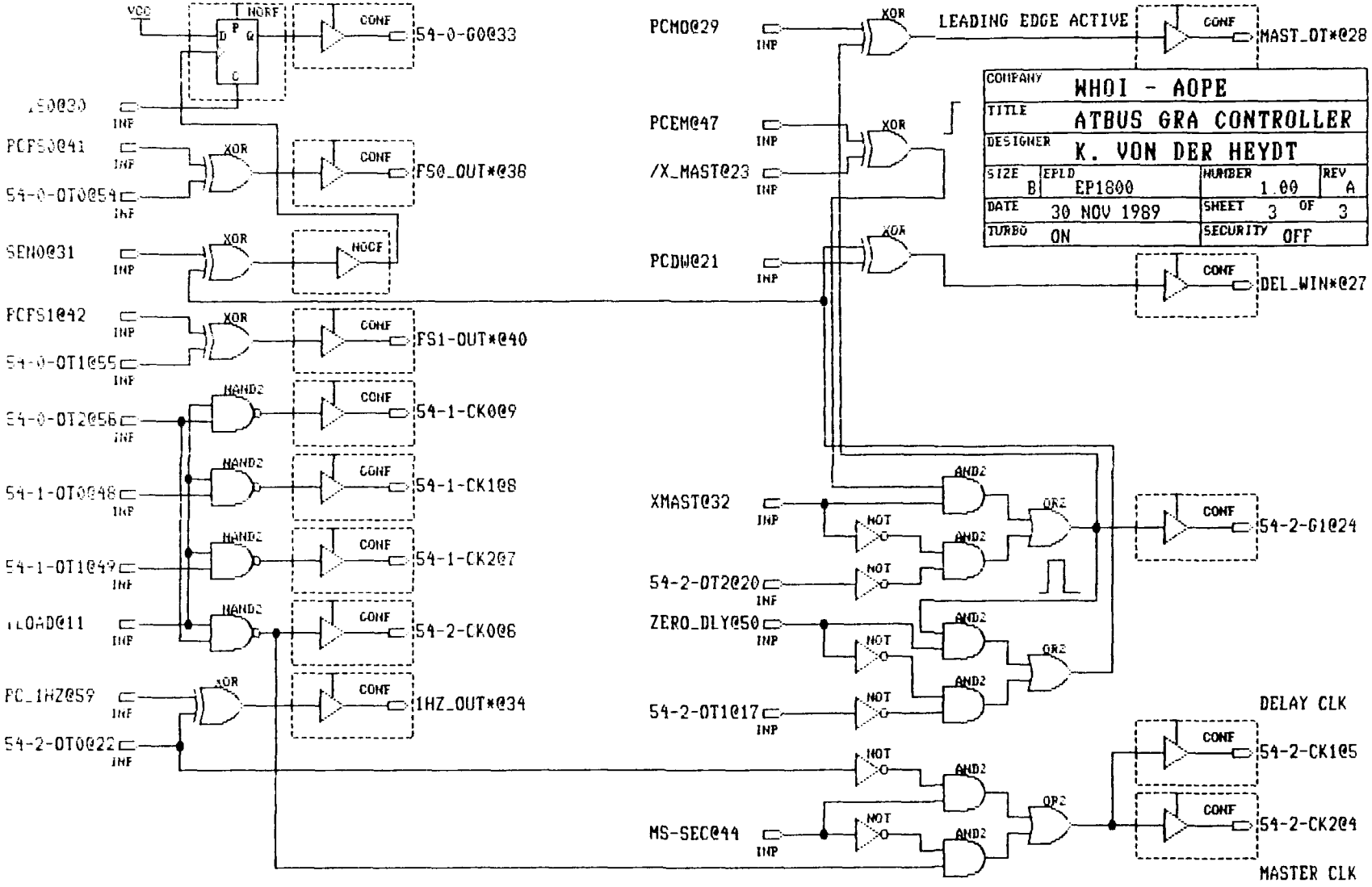


Figure 37. Altera PLD, Acquisition Parameter Control

```
PROJECT NAME  (type after colons)        :HEARD ISLAND

EXPERIMENT TYPE                         :TOMOGRAPHY
REFLECTION
REFRACTION
AMB NOISE
REVERBERATION
CW
TEST
etc...

EXPERIMENT #                            :00

OPTICAL DISK S/N  (<=15 chars)          :22812-1

SAMPLE RATE IN HERTZ (a float)          :228

LATITUDE-north (DEGREES,MINUTES,SECONDS)        :35,41,07
LONGITUDE-west (DEGREES,MINUTES,SECONDS)        :123,02,53

Preamp Gain.... (linear)                 2
Low Pass Filter Cutoff                  80


TOTAL # CHANNELS                        :32


CHANNEL TYPE POSSIBILITIES...input type number
1=HARDWIRED HYDROPHONE
2=ANALOG TELEMETRY HYDROPHONE
3=DIGITAL TELEMETRY HYDROPHONE
4=GEOPHONE
5=ACCELEROMETER X AXIS
6=ACCELEROMETER Y AXIS
7=ACCELEROMETER Z AXIS
8=
9=
10=

TYPE ACCORDING TO ABOVE LIST
SENSITIVITY SHOULD BE IN DBV RE 1 uP/HZ....
! DEPTH GIVEN IN METERS
! FILTER SETTINGS GIVEN IN HERTZ
! FILTER ROLLOFF'S GIVEN IN -DB/OCT
! FIXED GAIN GIVEN BY LINEAR FACTOR
! AMPLIFIER TYPE --  1 = NEW GRA, 0 = OLDGRA
! GRA CHANNEL # REFERS TO GRA CARD ADDRESS
! CH  IN FIRST COLUMN REFERS TO RECORDED FILE CHANNEL #


! TO SELECT A GIVEN CHANNEL FOR USE, INSTALL AN ASTERISK '*' IN PLACE
! OF THE UNDERSCORE '_' PRECEEDING THE CHANNEL #'S BELOW
! The high pass filtering consists of the single pole @ 10Hz of the sensor
! and the 4 pole Butterworth on the GRA.  There is an additional pole on the
! GRA in the form of an AC coupling @ about .03z after the LPF.  The buffer
! amp has an HP pole at about .03Hz as well if it is AC coupled.

:*00    A = TYPE         (as per above list)     :1
        B = SENSITIVITY  (dB re 1V/uPa/Hz)       :-170
        C = DEPTH        (meters)                :
        D = HPF @        (-6db pt, Hz)           :10
        E = HPF ROLLOFF  (-db/oct)               :30
        F = LPF @        (-3db pt, Hz)           :80
        G = LPF ROLLOFF  (-db/oct)               :48
        H = ONBOARD FIXED GAIN  (linear)         :2
        I = AMPLIFIER TYPE  (0=old, 1=new gra)   :1
        J = SENSOR/PATCH PANEL #                 :00
        K = EXTERNAL FIXED GAIN (linear)         :10
        This is the TOP sensor

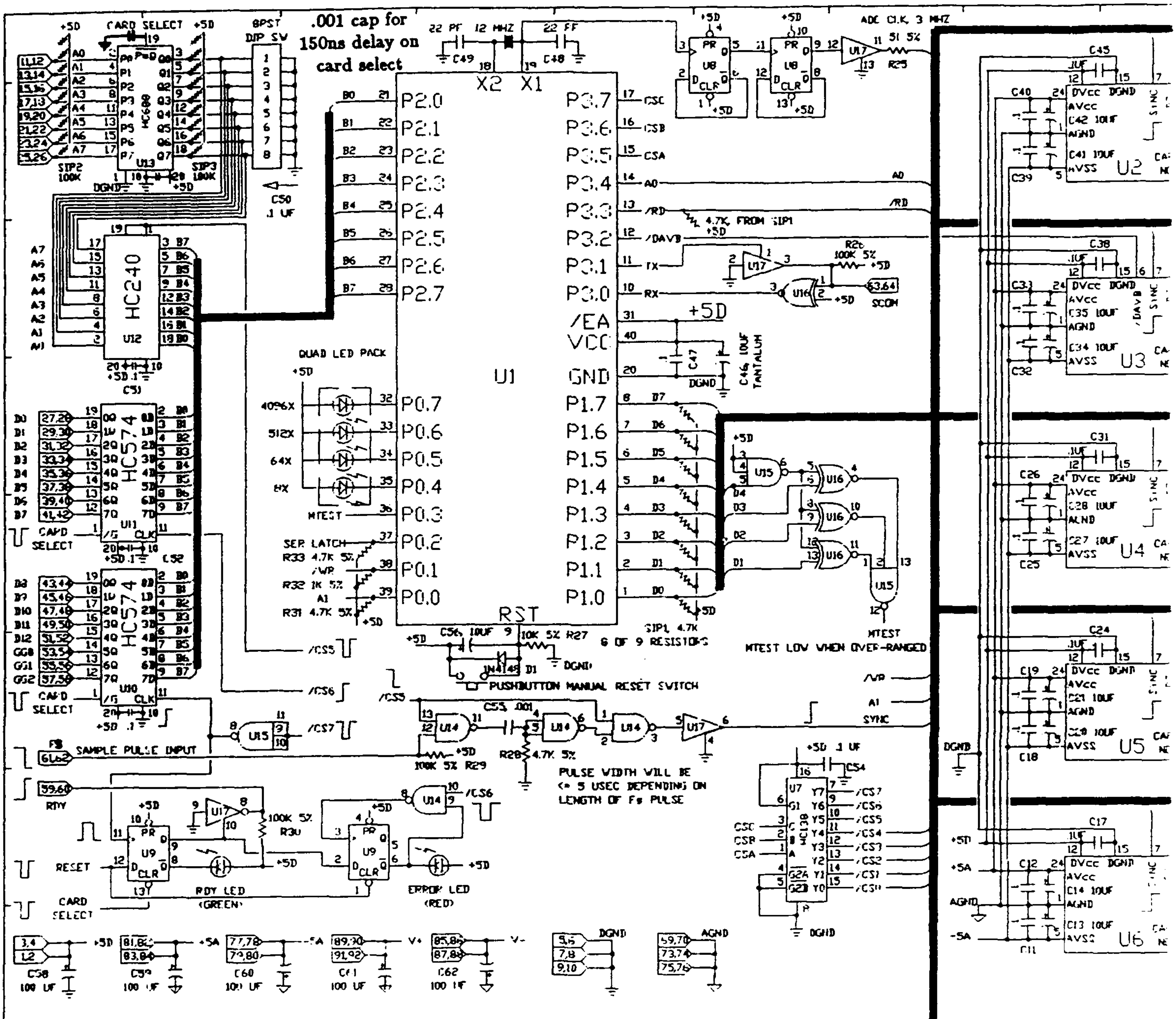
:*01    A       :1
        B       :-170
        C       :
        D       :10
        E       :30
        F       :80
        G       :48
        H       :2
        I       :1
        J       :01
        K       :10

:*02    A       :1
        B       :-170
        C       :
        D       :10
        E       :30
        F       :80
        G       :48
        H       :2
        I       :1
        J       :02
        K       :10

:*03    A       :1
        B       :-170
        C       :
        D       :10
        E       :30
        F       :80
        G       :48
        H       :2
        I       :1
        J       :03
        K       :10
                |
                |
                |
                |
                |

:*31    A       :1
        B       :-170
        C       :
        D       :10
        E       :30
        F       :80
        G       :48
        H       :2
        I       :1
        J       :31
        K       :10
```

Figure 38. Sample ASCII Data Header File Template



NOTES:

U1 & U17 ARE SOCKETED ALLOW SPACE FOR "ZIF" SOCKET FOR U1
U8, U9, U14, U15, U16, U17 HAVE .1UF DECOUPLING CAPS BETWEEN +5D AND DGND (C63 - C68)
U8 & U9 ARE HC74 PIN 7 = DGND, PIN 14 = +5D
U14 IS HC132 PIN 7 = DGND, PIN 14 = +5D
U15 IS HC10 PIN 7 = DGND, PIN 14 = +5D
U16 IS HC266 PIN 7 = DGND, PIN 14 = +5D
U17 IS HC125 PIN 7 = DGND, PIN 14 = +5D
FOR U23, U25 - U30, PIN 4 = V-, PIN 7 = V+ ; 8 PIN MINI DIPS
DATA TO HOST IS POS TRUE, 2'S COMPLEMENT, D12 IS SIGN BIT, D11 IS MSB
ADDRESS BYTE IS POS TRUE, I.E. ALL LOW = ADDRESS 00H
50/100 PIN EDGE CONNECTOR IS CONFIGURED AS FOLLOWS:

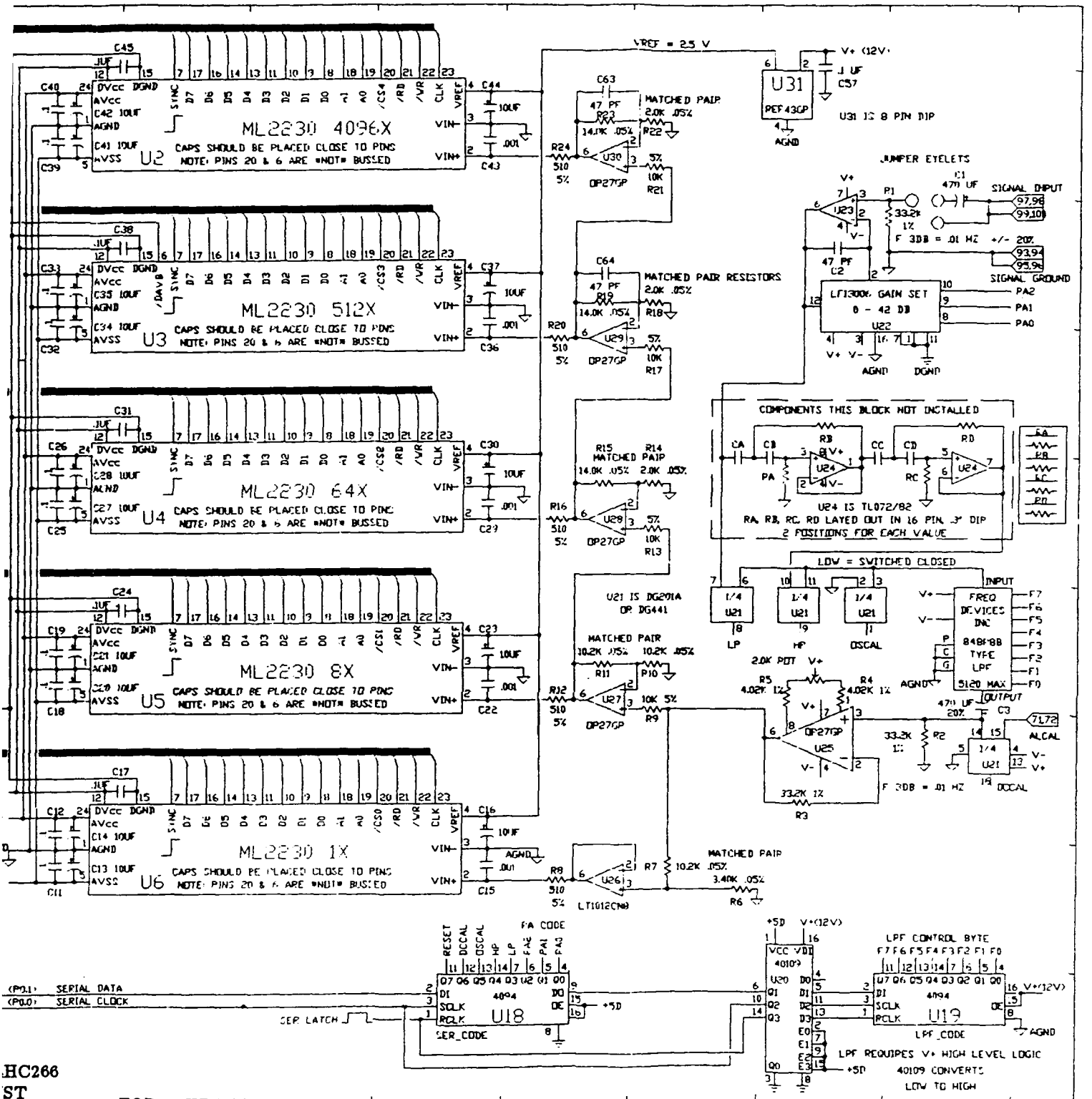
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47	49	51	53	55	57	59	61	63	65	67	69	71	73	75	77	79	81	83	85	87	89	91	93	95	97	99
2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	52	54	56	58	60	62	64	66	68	70	72	74	76	78	80	82	84	86	88	90	92	94	96	98	100

U16 MUST BE NATIONAL SEMICONDUCTOR 74HC266 OR ANYBODY ELSE'S 74HC7266. GATES MUST HAVE "PUSH PULL" OUTPUTS, NOT OPEN DRAIN

FOR 10

Ra = 17.23 Ko
Rb = 14.70 Ko
Rc = 41.59 Ko
Rd = 6.09 Ko

Figure 40. GRA Schematic



HC266
ST
TAIN

FOR 10 HZ HPF:

Ra = 17.23 Kohm (17.4k 1%)
Rb = 14.70 Kohm (14.7k 1%)
Rc = 41.59 Kohm (41.2k 1%)
Rd = 6.09 Kohm (6.04k 1%)

DEPARTMENT OF OCEAN ENGINEERING WOODS HOLE OCEANOGRAPHIC INSTITUTION		TITLE: CEAREX GPA	
CONTRACT: ARCTIC ACOUSTICS 10/161.02			
REVISION: REV. 12/88	DESIGN: KVDH	DRAWN: KVDH	DATE: 23 AUG 1988
SCALE:	DWG NO:	DWG FILE: GRA88	SHEET: 1 OF 1 | B

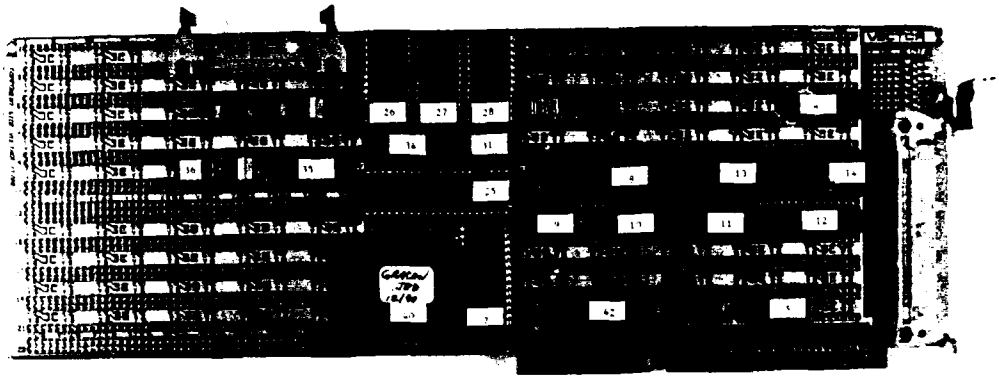


Figure 41. GRA Interface, 16 bit ISA Bus

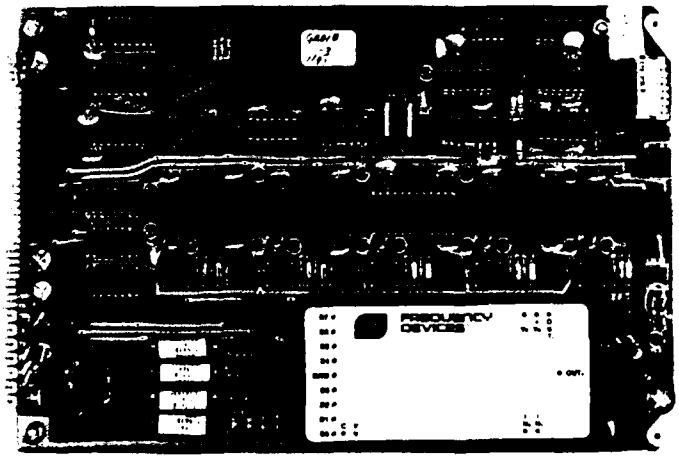


Figure 39. Gain Ranging Amplifier, (GRA), Single Channel

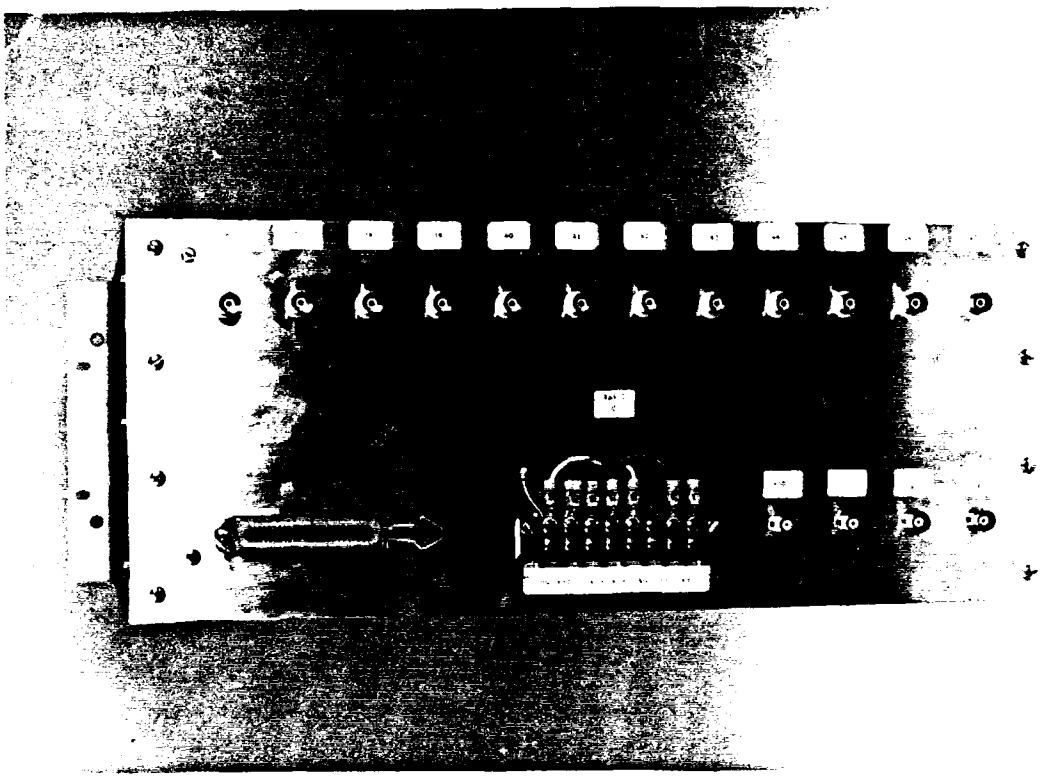


Figure 43. GRA Chassis rear panel showing isolated BNC signal inputs & Data/Control connector. Multiple chassis are bussed on 50 conductor ribbon cable.

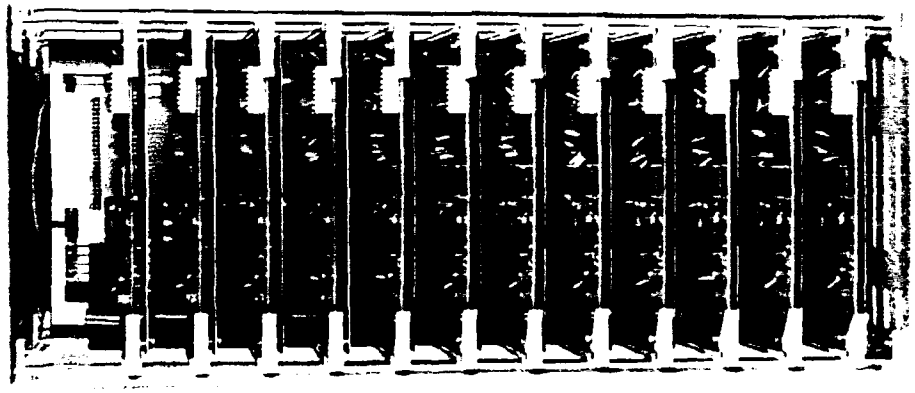


Figure 42. GRA Chassis Front, 12 Channels

Appendix A

The following is a description of the "sequencer code" that is created by the acquisition program in preparation for data recording using the GRA. Each of the sequencer output lines can be thought of as a digital control for a data generating device.

A 1k by 18 bit FIFO buffers data from the GRA's. This FIFO can easily be expanded if necessary. When the RDY line goes active, all channels are stored to this FIFO at a rate of 8 BCLK cycles per transfer. A BCLK cycle on a standard ISA bus is 8 MHz although on some machines this rate can be altered. SCLK=BCLK/2 is used to clock another 1k by 18 FIFO which stores the sequencer code. Four SCLK cycles are used to permit the flexibility to acquire data from other devices (like the old GRA's which require a "read clock" toggle per channel). Standard 120 ns FIFO's are fast enough for BCLK $\leq$ 12 Mhz. For BCLK = 16 Mhz, 80 ns FIFO's should be used. If old GRA channels are to be accessed, the upper 2 channel address bits are used to enable the chassis and CH ADRS bit 0 is used as the RD CLK, on neg going edge.

- Sequencer bit 0, DATA-WR, active lo, causes write to data FIFO
- Sequencer bit 1, LC-CHK, active hi, writes bit 17 of data FIFO to indicate that the tagged channel is the last in the sequence so acq prog can check for synchronization at end of buffers
- Sequencer bit 2, RDY-RST active hi, resets RDY FF when data for last channel is stored
- Sequencer bit 3, KILL-CLK, active hi, clears SCLK FF and holds sequencer FIFO in reset condition
- Sequencer bit 4 not used, extra ch adrs?
- Sequencer bit 5 not used, extra ch adrs?
- Sequencer bit 6 not used
- Sequencer bit 7 not used

Note, that in the quiescent state the sequencer output latch buffer holds the control and channel address data from the last state.

seqbit7	seqbit6	seqbit3	seqbit4	seqbit3	seqbit2	seqbit1	seqbit0
				KILL_CLK	RDY_RST	LC_CHK	DATA_WR

single ch	low byte	high byte	
SEQ ADRS	CH_ADRS	CTRL_BYTE	FUNCTION
''STATE''	msb lsb	msb lsb	
	1111 1111	0000 1001	QUIESCENT STATE
0	0000 0000	0000 0001	all control bits inactive

```
1          0000 0000     0000 0001   all control bits inactive
2          0000 0000     0000 0110   RDY_RST, LC_CHK active, DATA_WR active
3          1111 1111     0000 0111   RDY_RST, LC_CHK active, DATA_WR inactive
4          1111 1111     0000 1001   KILL_CLK active; DATA_WR, RDY_RST, LC_CHK
                                     inactive
```

```
Sequencer ram address = (ch# * 4) + n   where n = 0 thru 3
In the case of single ch, last channel mode is always used.
```

```
SEQ ADRS    CH_ADRS      CTRL_BYTE   FUNCTION   (for > 1 channel)
''STATE''
            1111 1111    0000 1001   QUIESCENT STATE
0             CH 0       0000 0000   all control bits inactive
1             CH 0       0000 0001   all control bits inactive
2             CH 0       0000 0000   DATA_WR active
3             CH 1       0000 0001   all control bits inactive

4             CH 1       0000 0001   all control bits inactive
5             CH 1       0000 0001   all control bits inactive
6             CH 1       0000 0000   DATA_WR active
7             CH 2       0000 0001   all control bits inactive
               |              |        *
               |              |
               |              |
last-4      last CH      0000 0001   all control bits inactive
last-3      last CH      0000 0001   all control bits inactive
last-2      last CH      0000 0110   DATA_WR, RDY_RST, LC_CHK active
last-1     1111 1111     0000 0111   RDY_RST, LC_CHK active, DATA_WR inactive
last       1111 1111     0000 1001   KILL_CLK active, others inactive
```

An unused channel address must be forced onto the upper byte of the sequencer word to insure no conflicts on the GRA data lines if GRA's are connected. CH ADRS is in the upper byte of the sequencer word. CONTROL bits are in the lower byte. The following "C" routine is used to load the sequencer and create the "state machine" code that interrogates the GRA's and loads data from them into the FIFO buffer.

```
void setup_sequencer(void)
{
  int i;

/* toggle KILL_CLK so control FF Q is known to be set */
  outportb(IOPC,(pc&=0xf7)); /* HOST_CON lo */
  outportb(IOPC,(pc&=0xfd)); /* reset sequencer and data fifo's */
  outportb(IOPC,(pc|=0x02));

/* want to make sure of state of KILL_CLK ff */
/* address to 'ff' so that ch 0 is disabled  */
  outport(SEQW,(0xff01)); /* load sequencer with a lo/hi for KILL_CLK */
```

```
  outport(SEQW,(0xff0d)); /* and RDY_RST  */
  inportb(SEQR); inportb(SEQR); /* read out these 2 words from sequencer */
  outportb(IOPC,(pc&=0xfd)); /* reset sequencer and data fifo's */
  outportb(IOPC,(pc|=0x02));

/* setup sequencer */
#define S0      0x01 /* sequencer codes */
#define S1      0x01
#define S2      0x00
#define S3      0x01
#define S2L     0x06
#define S3L     0x07
#define S4L     0x09

/* in QUIESCENT state, sequencer latches hold "1111 1111 0000 1000" */

  for(i=0;i<rh.ch;i++) /* load sequencer with standard acq code */
  {
    outport(SEQW,((ch[i]<<8)|S0));  inportb(SEQR); /* latch has S0 */
    outport(SEQW,((ch[i]<<8)|S1));  inportb(SEQR); /* latch has S1 */
    if((i+1)==rh.ch)  /* last channel */
    {
      outport(SEQW,((ch[i]<<8)|S2L));  inportb(SEQR); /* latch has S2L */
      outport(SEQW,((0xff<<8)|S3L));   inportb(SEQR); /* latch has S3L */
      outport(SEQW,((0xff<<8)|S4L));   inportb(SEQR); /* latch has S4L */
    }
    else  /* this isn't the last channel */
    {
      outport(SEQW,((ch[i]<<8)|S2));   inportb(SEQR);   /* latch holds S2 */
      outport(SEQW,(((ch[i+1])<<8)|S3));  inportb(SEQR);/* latch holds S3 */
    }
  }

/* last control word resets sequencer read adrs to 0 and disables SCLK FF */
  inportb(SEQ_RT);              /* reset sequencer read pointer to adrs 0 */
  outportb(IOPB,(pb|=0x20));    /* enable pos edge RDY, HOST_CON still lo */
}
```

Appendix B

The following "C" routine has been used to convert the stored 2-byte floating point format to native single precision floating point. Data that has been exported in "TAR" and "image" copies on Exabyte 8mm tape are in this raw format. Many machines will have to read the raw data as bytes and transpose the upper and lower bytes of a value before they can use this routine. The low byte followed by high byte format of a short integer is not standard with all machines.

```
/* normize.c .........A routine to normalize 2-byte raw data samples,
GRA gain in the upper 3 bits of the integer and the lower 13 bits are the
selected ADC output.  The gain and mantissa bits are gnd true.  The mantissa
is 2's complement with bit 12 (msb) the sign bit.  This format is same as
for the old and new GRA's.  The fixed gain of the GRA preamp is accommodated.
The bit assignments are as follows:\\
*    bit 15    GRA bit 2  (msb, gain)
*    bit 14    GRA bit 1
*    bit 13    GRA bit 0  (lsb, gain)
*    bit 12    ADC bit 12 (sign bit, ADC)
*    bit 11    ADC bit 11 (msb, mantissa, ADC)
*    bit 10    ADC bit 10
*    bit 9     ADC bit 9
*    bit 8     ADC bit 8
*    bit 7     ADC bit 7
*    bit 6     ADC bit 6
*    bit 5     ADC bit 5
*    bit 4     ADC bit 4
*    bit 3     ADC bit 3
*    bit 2     ADC bit 2
*    bit 1     ADC bit 1
*    bit 0     ADC bit 0 (lsb, mantissa, ADC)

The function performed is:
          normalized value = (raw value<<3) * 10v / 4096 / 8 / gain / pag
          where ''gain'' = ranged gain
          and  ''pag'' = preamplifier fixed gain
*/

void normize(bufin,bufout,npts,pag)
unsigned short *bufin;
float *bufout;
short npts,pag;
{
  int i,mantissa;
  unsigned gain;

  if(pag==1)
  {
    for(i=0;i<npts;i++)
    {
      mantissa = (int)(~bufin[i] << 3);
```

```
      gain = (~bufin[i] & 0xe000);
      switch(gain)
      {
        case(0x8000): /* gain = 4096 */
        bufout[i] = 7.4505805e-8 * mantissa;
        break;
        case(0x6000):   /* gain = 512 */
        bufout[i] = 5.9604644e-7 * mantissa;
        break;
        case(0x4000): /* gain = 64 */
        bufout[i] = 4.7683715e-6 * mantissa;
        break;
        case(0x2000):  /* gain = 8 */
        bufout[i] = 3.8146972e-5 * mantissa;
        break;
        case(0x0000): /* gain = 1 */
        bufout[i] = 3.0517578e-4 * mantissa;
        break;
        default: /* bogus gain value */
        bufout[i] = 0.0;
        break;
      }
    }
  }
  else
  {
    for(i=0;i<npts;i++)
    {
      mantissa = (int)(~bufin[i] << 3);
      gain = (~bufin[i] & 0xe000);
      switch(gain)
      {
        case(0x8000): /* gain = 4096 */
        bufout[i] = 7.4505805e-8 * mantissa/pag;
        break;
        case(0x6000):   /* gain = 512 */
        bufout[i] = 5.9604644e-7 * mantissa/pag;
        break;
        case(0x4000): /* gain = 64 */
        bufout[i] = 4.7683715e-6 * mantissa/pag;
        break;
        case(0x2000):  /* gain = 8 */
        bufout[i] = 3.8146972e-5 * mantissa/pag;
        break;
        case(0x0000): /* gain = 1 */
        bufout[i] = 3.0517578e-4 * mantissa/pag;
        break;
        default: /* bogus gain value */
        bufout[i] = 0.0;
        break;
      }
    }
  }
}
```

Appendix C

SAMPLE DISK HEADER SECTOR.....1024 bytes at BLOCK 000000

```
000  4f 44 48 44 31 35 32 32 37 00 00 00 00 00 00 00  ODHD15227.......
010  00 00 00 00 c6 07 15 09 21 0a 3d 1b 3f 42 0f 00  ................
020  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
030  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
040  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
050  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
060  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
070  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  .... ............
080  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
090  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
0a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
0b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
0c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
0d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
0e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
0f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
100  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
110  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
120  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
130  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
140  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
150  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
160  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
170  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
180  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
190  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
1a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
1b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
1c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
1d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
1e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
1f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
200  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
210  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
220  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
230  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
240  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
250  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
260  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
270  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
280  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
290  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
2a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
2b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  .... ............
2c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
2d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
2e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
2f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
300  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
310  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
320  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
330  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
340  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
350  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
360  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
370  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
380  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
390  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
3a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
3b0  00 00 00 00 00 00 cc 00 00 00 00 00 00 00 00 00  ................
3c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
3d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
3e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ................
3f0  00 00 00 00 00 00 00 00 00 00 00 00 00 4f 44 48  .............ODH
```

Appendix D

SAMPLE OPTICAL DISK DIRECTORY ENTRY SECTOR....1024 bytes

```
000  4f 44 49 52 74 65 73 74 30 00 00 00 00 00 00 00   ODIRtest0.......
010  00 00 00 00 c6 07 15 09 2a 0a 38 31 3e 42 0f 00   ........*.81>B..
020  01 00 00 00 00 8c 2b 01 02 00 00 00 e3 4a 00 00   ......+......J..
030  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
040  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
050  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
060  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
070  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
080  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
090  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
100  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
110  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
120  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
130  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
140  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
150  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
160  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
170  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
180  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
190  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
200  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
210  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
220  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
230  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
240  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
250  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
260  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
270  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
280  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
290  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
300  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
310  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
320  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
330  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
340  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
350  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
360  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
370  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
380  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
390  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3f0  00 00 00 00 00 00 00 00 00 00 00 00 4f 44 49 52   ............ODIR
```

Appendix E

SAMPLE DATA RECORD HEADER SECTOR....1024 bytes

```
000  44 41 54 41 78 78 78 00 00 00 00 00 00 00 00 00   DATAxxx.........
010  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
020  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
030  00 00 00 00 00 00 c6 07 08 01 82 02 75 03 0c 00   ................
040  00 00 00 a8 00 00 00 40 9c 46 f1 03 00 00 00 00   ................
050  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
060  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 14   ................
070  00 14 00 14 00 14 00 14 00 14 00 14 00 14 00 14   ................
080  00 14 00 14 00 14 00 00 00 00 00 00 00 00 00 00   ................
090  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
100  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
110  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
120  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
130  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
140  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
150  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
160  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
170  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
180  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
190  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
1f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
200  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
210  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
220  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
230  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
240  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
250  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
260  00 00 00 00 00 00 00 00 00 00 00 00 00 00 05 00   ................
270  d8 02 00 00 01 00 32 00 00 00 00 00 00 00 00 00   ......2.........
280  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
290  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
2f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
300  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
310  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
320  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
330  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
340  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
350  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
360  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
370  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
380  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
390  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
3f0  00 00 00 00 00 00 00 00 00 00 00 00 44 41 54 41   ............DATA
```

Appendix F

SAMPLE FIRST DATA SECTOR IN A FILE....1024 bytes

```
000  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ................
010  ff ff ff ff ff ff ff ff fe ff ff ff fe ff fe ff  ................
020  fe ff ff ff ff ff ff ff df ff ff ff fe ff fe ff  ................
030  ff ff ff ff fd ff fe ff fe ff ff ff ff ff ff ff  ................
040  df ff fe ff fe ff ff ff ff ff ff ff fe ff fe ff  ................
050  ff ff ff ff fe ff fe ff df ff ff ff ff ff ff ff  ................
060  ff ff ff ff ff ff fe ff fe ff ff ff fe ff ff ff  ................
070  e1 ff ff ff fe ff ff ff 5a 60 e5 7f 18 60 01 60  ........Z`..`.`.
080  53 60 19 60 f2 7f 31 60 4f b8 c0 7f 63 7f c7 7f  S`.`..1`O...c...
090  0f 60 6c 7f cc 7f b7 7f 0a 7f 2e 7f 75 7f 03 60  .`l.........u..`
0a0  f4 b7 4f 7f 5e 7f 37 7f 83 7f d4 7e 1a 7f b8 7e  ..O.^.7....~...~
0b0  45 7e 72 7e 7a 7e f6 7f c1 b7 90 7e 92 7e 2f 7e  E~r~z~.....~./~
0c0  61 7f 92 7e 2f 7f f0 7e 62 7e 8e 7e 56 7e b7 7f  a..~/..~b~..~V~..
0d0  f1 b7 69 7e 1e 7e 05 7e 66 7f 0b 7f 87 7f 89 7e  ..i~.~.~f......~
0e0  4a 7e d8 7e 5f 7e df 7f 0b b8 02 7e 73 7d b1 7d  J~.~_~.....~s}.}
0f0  e2 7e de 7e 3e 7f 14 7e 71 7d 72 7d 50 7d e5 7f  .~.~>..~q}r}P}..
100  eb b7 c4 7d 09 7d 28 7d b5 7e 02 7e f2 7d ce 7c  ...}.}(}.~.~.}.|
110  4e 7c 2d 7c 80 7c 9b 7f de b7 84 7c 67 7c 2a 7c  N|-|.|.....|g|*|
120  c1 7e 40 7d 3e 7d dd 7c f9 7b c8 7b 62 7b 74 7f  .~@}>}.|.{.{b{t.
130  ea b7 fc 7a 0d 7b d7 7a ea 7e 7a 7d 6e 7d 4e 7d  ...z.{.z.~z}n}N}
140  e5 7b 55 7c 28 7b 53 7f ee b7 86 7a 27 7a 5a 7a  .{U|({S....z'zZz
150  de 7e 09 7e ec 7d 68 7d 60 7c 59 7c c6 7b 12 7f  .~.~.}h}`|Y|.{..
160  db b7 ac 7a 32 7a 96 7a a8 7e cb 7d f1 7d 2f 7d  ...z2z.z.~.}.}/}
170  3d 7c 0e 7c 0b 7c a3 7f d6 b7 0c 7b ea 7a f4 7a  =|.|.|.....{.z.z
180  3a 7e 4f 7d b0 7d 09 7d 8b 7c 14 7c b4 7b 03 60  :~O}.}.}.|.|.{.`
190  e6 b7 28 7b e9 7a 34 7b 78 7e 2f 7d a7 7d e1 7c  ..({.z4{x~/}.}.|
1a0  a3 7c 40 7c e8 7b 41 60 f6 b7 c9 7a de 7a 2e 7b  .|@|.{A`...z.z.{
1b0  88 7e 8c 7d d7 7d d1 7c 4d 7c f0 7b 0e 7c f5 7f  .~.}.}.|M|.{.|..
1c0  f4 b7 cf 7a dd 7a 00 7b 8a 7e b0 7d 8b 7d f1 7c  ...z.z.{.~.}.}.|
1d0  44 7c 90 7c 20 7c 1b 60 0f b8 75 7b 0e 7b 26 7b  D|.|.|.`..u{.{&{
1e0  85 7e 97 7d 8e 7d 41 7d 67 7c 7f 7c ff 7b 20 60  .~.}.}A}g|.|.{ `
1f0  20 b8 c1 7b 49 7b 35 7b 56 7e b4 7d 96 7d 15 7d  ..{I{5{V~.}.}.}
200  a2 7c 5e 7c 12 7c 12 60 0e b8 ba 7b 1b 7b 74 7b  .|^|.|.`...{.{t{
210  33 7e b8 7d 49 7d d4 7c a3 7c 77 7c 37 7c 3a 60  3~.}I}.|.|w|7|:`
220  08 b8 86 7b 3e 7b a5 7b 2a 7e b7 7d 05 7d 31 7d  ...{>{.{*~.}.}1}
230  80 7c 69 7c b0 7c 68 60 15 b8 0a 7c a1 7b be 7b  .|i|.|h`...|.{.{
240  e7 7d 8a 7d 59 7d 4e 7d 0d 7d 80 7c 8f 7c c4 60  .}.}Y}N}.}.|.|.`
250  19 b8 24 7c e9 7b d5 7b fc 7d 3f 7d ce 7d 5f 7d  ..$|.{.{.}?}.}_}
260  16 7d be 7c 33 7c 3b 60 19 b8 db 7b a0 7b 27 7c  .}.|3|;`...{.{'|
270  c8 7d 14 7d d4 7d 4c 7d f0 7c 29 7c 75 7c d7 60  .}.}.}L}.|)|u|.`
280  20 b8 ff 7b ac 7b 0b 7c 81 7d 79 7d 35 7d 4a 7d  ...{.{.|.}y}5}J}
290  76 7d 79 7c 5a 7c 85 60 29 b8 a9 7c ce 7b e8 7b  v}y|Z|.`)...|.{.{
2a0  a4 7d ad 7d 98 7d 61 7d 77 7d 5c 7c 91 7c 2d 60  .}.}.}a}w}\|.|-`
2b0  24 b8 8b 7c 14 7c f9 7b 0c 7e 69 7d e7 7d 44 7d  $..|.|.{.~i}.}D}
2c0  ce 7c 4b 7c 80 7c b7 60 0b b8 aa 7b 2b 7c 3b 7c  .|K|.|.`...{+|;|
2d0  bb 7d 59 7d a2 7d 6e 7d b9 7c 2f 7c 5a 7c c7 60  .}Y}.}n}.|/|Z|.`
2e0  ea b7 5c 7c 10 7c 3b 7c a6 7d 8c 7d d2 7d 30 7d  ..\|.|;|.}.}.}0}
2f0  45 7d 9e 7c 9f 7c cf 60 ec b7 e2 7c 84 7c 21 7c  E}.|.|.`...|.|!|
300  8d 7d 0b 7d 9c 7d 0b 7d 68 7d d8 7c ec 7c 93 60  .}.}.}.}h}.|.|.`
310  01 b8 89 7c 31 7c 8c 7c cb 7d 66 7d 7e 7d 5f 7d  ...|1|.|.}f}~}_}
320  0c 7d f7 7c c9 7c d2 60 02 b8 79 7c 77 7c 9a 7c  .}.|.|.`..y|w|.|
330  e2 7d 4c 7d 54 7d 72 7d 46 7d 69 7c ce 7c ce 60  .}L}T}r}F}i|.|.`
340  f6 b7 e1 7c 76 7c b1 7c 0f 7e 93 7d a2 7d a1 7d  ...|v|.|.~.}.}.}
350  52 7d 86 7c ef 7c fe 60 ec b7 00 7d bb 7c e7 7c  R}.|.|.`...}.|.|
360  eb 7d c9 7d 04 7e 57 7d 2f 7d b8 7c 36 7d aa 60  .}.}.~W}/}.|6}.`
370  ea b7 e5 7c 84 7c a2 7c e0 7d 5f 7d 0f 7e 57 7d  ...|.|.|.}_}.~W}
380  1c 7d 95 7c b8 7c 5e 60 e5 b7 90 7c 5b 7c a1 7c  .}.|.|^`...|[|.|
390  fc 7d 49 7d ba 7d 47 7d 8f 7d ea 7c cb 7c 89 60  .}I}.}G}.}.|.|.`
3a0  df b7 92 7c cf 7c b3 7c a6 7d 57 7d d4 7d 75 7d  ...|.|.|.}W}.}u}
3b0  42 7d d8 7c 38 7d c1 60 e8 b7 16 7d d4 7c 00 7d  B}.|8}.`...}.|.}
3c0  90 7d ce 7d 2d 7e 93 7d c4 7c bf 7c 0c 7d d2 60  .}.}-~.}.|.|.}.`
3d0  e8 b7 f6 7c e2 7c a7 7c 6b 7d 8d 7d 14 7e 80 7d  ...|.|.|k}.}.~.}
3e0  c4 7c 8d 7c d0 7c bd 60 e3 b7 ec 7c a1 7c 6e 7c  .|.|.|.`...|.|n|
3f0  d0 7d 89 7d 14 7e 9f 7d 6a 7d 01 7d d3 7c d2 60  .}.}.~.}j}.}.|.`
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16. Abstract (Limit: 200 words)

Multichannel data acquisition has been a keystone of 7 ONR sponsored Arctic acoustic research programs conducted jointly by WHOI and MIT investigators from 1978 through 1989. This report describes the status and capability of the most recent system developed at WHOI for the purpose of acquiring digital data from up to 64 channels at sampling rates up to 20 kHz per channel with data bandwidth to 5120 Hz. ONR funded the development of and use of this system and its prototype for 2 Arctic field experiments, PRUDEX 87 and CEAREX 89. It was most recently used during the Heard Island Feasibility Experiment in February 1991. Of note are *the auto-gain ranging capability offering a dynamic measurement range of greater than 120 dB*, the continuous storage capability of up to 200,000 samples per second to a Small Computer System Interface (SCSI) device, typically optical disk, and easy expandability with additional identical channels connected in parallel.

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